OPTIMIZATION OF LOW VOLTAGE CHARGE PUMP WITH STACKING POWER GATING

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ABSTRACT

A low voltage six stage two branch charge pump with stacking power gating technique is developed to help start up a step-up converter in energy harvesting applications. In this paper, a comparative analysis of high performance stacking power gating schemes is applied to the charge pump circuit, so it minimizes the leakage power and leakage voltage. The innovative power gating schemes such as stacking power gating, CMOS startup charge pump based stacking power gating are first utilize backward control scheme and two branch operation. The combination of backward control scheme and two branch operation allows the charge transfer switches to completely turned on and off. In further to evaluate the efficiency, the simulation has been done using such high performance power gating schemes. Finally it is observed that the leakage current in standby mode, the leakage power is reduced by the conventional power gating. The charge pump with stacking power gating circuit operates in 45nm technology. Under a 320mv supply the average power consumption of the circuit is minimized to approximately from $2.986 \times 10^{-3}$ watts to $1.457 \times 10^{-4}$ watts. This process has been performed using Tanner EDA tool.

Keywords: Six Stage Two Branch Charge Pump, Sub Threshold Operation, Stacking Power Gating, Leakage Power.

I. INTRODUCTION

In remote sensing applications, energy harvesting is often utilized to provide a renewable power source for sensor nodes. Some energy harvesting sources are characterized with very low voltage output, which prevents their immediate usage [1]. Meanwhile, most sensors require high operating voltage in several volts. To solve this problem, a stacking power gating technique in CMOS Startup charge pump for energy harvesting step-up converter can be used to boost a low voltage source to high voltage source and provides a high output power to load.

However, for operating a stacking power gating in step-up converter at charge pump under a low voltage supply is always challenging [2]. In steady state operation, a step-up converter can use its own high voltage output power, but a sufficiently high voltage must be applied to start up the system by using the stacking power gating technique. In the reported energy harvesting systems it can operate from dozens of mill volts, but it needs external high voltage sources or expensive mechanical active devices to start up the system, which limits their practical application. So that only we are modified in that by means of stacking power gating. Apparently, a better approach will be build an integrated startup charge pump with stacking power gating, which can generate a high-voltage pulse to bootstrap a step-up converter from a low voltage input [8].
In this paper, a power gating of startup charge pump is proposed for low voltage and low power operation. The charge pump with an integrated ring oscillator utilizes sub threshold operation and body bias technique used to enable startup and operate under a low voltage supply. The charge pump is the first utilized both backward control scheme and two branches of Charge Transfer Switches (CTSs) to direct charge flow. The backward control scheme uses the internal boosted voltage for dynamically control the CTS’s gate, and the two branches utilize both NMOS and PMOS to implement their switching structure. With a special structure of stacking power gating in CMOS startup charge pump obtains performance improvement in some of the key specifications. A startup charge pump only works during the startup period of a step-up converter, and it supports a capacitive load [2].

The rest of this paper is organized as follows. Section II surveys all of the previous works with CMOS startup charge pump in step up converters. Section III describes the concepts of stacking power gating. In Section IV describes the proposed system stacking power gating with startup charge pump. In section V, simulation output waveforms are shown and the comparisons of previous charge pumps are tabulated. The proposed stacking power gating with charge pump offers best performance at minimum supply voltage, pumping efficiency, charge transferability and capacitance drivability.

II. CMOS START-UP CHARGE PUMP IN STEP-UP CONVERTERS

The startup low voltage six-stage two branch charge pump is designed for low voltage power supply applications was implemented with two CTSs branches and compensated structure in each stage [1]. Two compensated branches are used to transfer charge significantly improves pumping efficiency and reduce output ripples, because two pumping branches can provide better charge transferability.

In very large devices there is no need for designing the CTSs, which can lower the effect of the device size on the threshold voltage. Meanwhile, the redistribution loss between the last stage and the output capacitor can be reduced, since one of the two branches are always provide current to keep the output voltage stable.

A charge pump was designed for low voltage power supply applications; the beginning is to build a ring oscillator which can generate out of phase clock signals. The oscillator must able to work under a voltage supply of several hundred millivolts. It should have a rail-to-rail output swing and the output current drivability should be large. In 0.18µm process, the absolute threshold voltage of a transistor is around 500mv. If the voltage supply is around 0.3V, the device must be operated in sub threshold region. The five stage sub threshold ring oscillator, body bias ring oscillator with two buffer stages are used to operate the inverter in sub threshold region. Two phase shifting circuits with large size buffers are used to improve the clock output swing and the current drivability because the clock generator has to drive a total pumping capacitance.

A. Six stage two branch charge pump

The input startup voltage of the proposed charge pump circuit is 320mv, it consists of 6 stages each stage having both upward and downward capacitor. Fig. 1. (a) and (b) shows the circuit diagram and waveform representation of proposed six stage two branch charge pump.
The proposed six stage charge pumps have two branches as shown above, if branch A and branch B employ internally boosted high voltages for backward dynamic control. Branch A consists of NMOSs (MN1-MN6), PMOSs (MP1-MP6), capacitors (C1-C6), inverters (INV1-INV5) and output control stage N1 and P1. Branch B consists of NMOSs (MN7-MN12), PMOSs (MP7-MP12), capacitors (C7-C12), inverters (INV6-INV10) and output control stage N2 and P2. All the NMOS’s bulks are connected to the source in deep n-well region except MN6 and MN12, the bulks of all devices constructing the inverters are connected to their sources [1].

The proposed charge pump is designed in 0.18μm CMOS process, under a 320mv supply the measured output voltage of the charge pump can rises from 0 to 2.04V and the average power consumption is $2.986160 \times 10^{-3}$ watts. Compared with other charge pumps design, the proposed charge pump has the highest charge transferability, the largest capacitance drivability and the highest pumping efficiency. in this process, a smaller threshold voltage can be achieved by reducing the width-to-length ratio of the device.

Advantages of the six stage two branch charge pump is in given as,

1. The last stage of the two branches are modified more effectively the CTSs should be turn on/off under low voltage supply.

2. In a standard CMOS process the two out of phase clock signals are generated under a low voltage supply.

3. Two compensated branches to transfer charge significantly, improve the pumping efficiency and reduce output ripples.

Fig. 1. (a). Six stage two branch charge pump circuit (b).Corresponding waveforms

III.STACKING POWER GATING TECHNIQUE

Power gating is a technique used in integrated circuit design to reduce power consumption, by shutting off the current to blocks of the circuit that are not in use. Internal stacking power gating is more suitable to shut off the block for small intervals of time. Power can be controlled by stacking power gating controllers and to provide power to the circuitry CMOS switches are used.
The power gated outputs block discharges slowly. Hence voltage levels of the output block spend more time in threshold voltage level (Vth), so it leads to larger short circuit current in the circuit.

![Stacking Power Gating Technique](image)

**Fig. 2. Stacking Power Gating Technique**

Low-leakage PMOS transistors are used as header switches to shut off power supplies, the stacking Power Gating parts of a design in the mode of sleep or standby. NMOS footer switches can also be used as sleep transistors in the design of stacking power gating technique. The sleep transistors can be inserting to splits the chip's power network into a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off. By using of cell- or cluster-based (or fine grain) approaches or a distributed coarse-grained approaches stacking Power Gating can be implemented.

Power gating technique is widely used to significantly suppress the leakage currents in standby mode. Stacking sleep transistors are used in stacking power gating technique to reduce the magnitude of peak current and voltage glitches in power rails (i.e) ground bounce noise [7]. In the proposed power gating technique, if stacking power gating scheme works on two strategies. (1) Reduction of leakage current by stacking effect, (2) Reductions of ground bounce noise by controlling the intermediate node voltage. In the technique stacking effect is used to reduce the leakage current.

**IV. PROPOSED SYSTEM**

The stacking power gating scheme is the most efficient way for reducing leakage power in standby mode. In this process we are using large transistors called sleep transistors, in series with the pull-up and pull-down stacks to cut-off the power supply rail from the circuit when the circuit is in standby mode. Ground bounce noise is an important issue in the design of nanometer circuits and this inductive noise is also associated with clock gating. Previous work we are design six stage two branch charge pump circuit in startup voltage but it consumes more power. Nowadays power is the most difficult, so stacking power gating scheme included for charge pump circuit it will reducing the leakage power. The proposed system of six stage two branch charge pump with stacking power gating are shown Fig. 3, the stages are designed by only using NMOS.

The clock signals clk and clkb are generated by the clock generator, if clk and clkb are two out of

![Fig. 3. Six stage two branch charge pump with stacking power gating technique](image.png)
phase clock signals. The charge from the power source is pushed into first branch, the loss between the last stage and the output capacitor will be charged by using the power gating technique in our project. In first and second stage, the charge will be pumped at normally in charge pump circuit by means the PMOS and NMOS transistors are connected header and footer switches to turn off mode but we apply the power gating technique the design in the mode of sleep or standby mode. When the next stages are turned off, the reverse charge sharing phenomenon may not be completely eliminated, reverse leakage can occur between adjacent nodes. So, to reduce leakage, longer channel length can be used by connecting the power gating technique will be increase the charge pumping efficiency.

Stacking power gating technique is applied for each stage of the charge pump design and each stage having the capacitive load of 2pF. The charge transfer switches in the circuit can be completely turned on and turned off, so its pumping efficiency is higher than that of the traditional design. Our proposed circuit is suitable for applications in low-voltage CMOS processes because of its high pumping efficiency and giving low power consumption.

IV. SIMULATION OUTPUT WAVEFORMS AND COMPARISON OF DIFFERENT CHARGE PUMPS

To achieve long term leakage stacking power reduction is an externally switched power supply is a very basic form of power gating.

Fig. 4. Waveform specifications of proposed system
TABLE I: Comparison of Different Charge Pumps

<table>
<thead>
<tr>
<th>Different Charge Pumps</th>
<th>Number of stages</th>
<th>Input voltage level</th>
<th>Power consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dickson charge pump</td>
<td>6</td>
<td>5V</td>
<td>3.394e-003 watts</td>
</tr>
<tr>
<td>Wu and Chang’s charge pump</td>
<td>6</td>
<td>5V</td>
<td>2.812e-003 watts</td>
</tr>
<tr>
<td>Linear charge pump</td>
<td>6</td>
<td>5V</td>
<td>3.036e-003 watts</td>
</tr>
<tr>
<td>Six stage two branch charge pump without stacking power gating</td>
<td>6</td>
<td>320mv to 5V</td>
<td>2.986e-003 watts to 2.419e-002 watts</td>
</tr>
<tr>
<td>Six stage two branch charge pump with stacking power gating</td>
<td>6</td>
<td>320mv to 5V</td>
<td>1.457e-004 watts to 1.220e-004 watts</td>
</tr>
</tbody>
</table>

V. CONCLUSION

A low voltage start-up six stage two branch charge pump with stacking power gating circuit is designed. The high performance stacking power gating structure has been presented for charge pump circuit which minimizes the leakage power and low voltage output in CMOS startup charge pump. Stacking power gating technique has been analyzed and the conditions for the important design objectives i.e. (i) Minimum leakage power (ii) Minimum low voltage output have been derived. As recent trend is towards the CMOS startup charge pump, if the stacking power gating technique is mostly used for reduction of leakage current. The stacking power gating technique reduces the leakage current less than compared to the conventional power gating structure. Under a 320mv supply the average power consumption of the circuit is minimized to approximately from 2.986e-003 watts to 1.457e-004 watts. In existing without stacking power gating technique is being achieved at cost of low performance in CMOS startup charge pump and power consumption of the process is high as 2.98e-003 watts. In further it will using another advanced VLSI process the power consumption of the circuit is (90%) reduced.

REFERENCES


