A Single Phase Multilevel Inverter with Novel Capacitor Voltage Balancing Technique

I. Gerald Christopher Raj, G. Praveenraj, M. Kaliammuorthy

Associate Professor, PG Scholar, Associate Professor,
Dept. of EEE, PSNA CET, Dindigul, India

E-Mail: gerald.gera@gmail.com, praveenrajmw@gmail.com, kaliasgoldmedal@gmail.com

December – 2015

www.istpublications.com
A Single Phase Multilevel Inverter with Novel Capacitor Voltage Balancing Technique

I. Gerald Christopher Raj, G. Praveenraj, M. Kaliamoorthy

Associate Professor, PG Scholar, Associate Professor,
Dept. of EEE, PSNA CET, Dindigul, India

E-Mail: gerald.gera@gmail.com, praveenrajmw@gmail.com, kaliasgoldmedal@gmail.com

ABSTRACT

For medium-voltage power electronic applications, multilevel converters have become a popular option. While conventional two-level converters utilize a direct series connection of switches to meet medium-voltage requirements, multilevel converters allow a higher voltage handling capability with reduced harmonic distortion and lower switching power losses. One of the most important requirements in the operation of multilevel converters is balancing capacitors voltages. They define all levels of the converter output voltage. However, the voltage across the capacitor may grow or decay so that the neutral point voltage fails to keep the half of the DC link voltage. They have a direct impact on the operation of the converters, as their variations are found on the voltages applied to the switching cells. This imbalanced condition needing higher rated capacitors and also can causes failure of the power semiconductors. The capacitors voltages must be equitably distributed to ensure a balanced distribution of the constraints in power switches voltage. This paper proposes a novel capacitor voltage balancing technique for multilevel inverter.

Index Terms- H-Bridge, Multilevel Inverter, Harmonics, PWM.

I. INTRODUCTION

Multilevel converters are mainly utilized to synthesis a desired 1- or 3-phase voltage waveform. The required multi-staircase output voltage is obtained by combining several dc voltage sources. Batteries solar cells, fuel cells & ultra-capacitors are the most common independent sources used. One of the important application of multilevel converters is focused on medium and high-power conversion. Nowadays, there are three commercial topologies of multilevel voltage-source inverters: neutral point clamped (NPC), cascaded H-bridge (CHB), and flying capacitors (FCs). Among these inverter topologies, cascaded multilevel inverter provides the higher output voltage and power levels (13.8 kV, 30 MVA) and the higher reliability due to its modular topology.

Diode-clamped multilevel converters are used in conventional high-power ac motor drive applications like conveyors, fans, pumps and mills. They are also utilized in metals, oil, gas, metals, mining, marine, water and chemical industries. They are also used in a back-to-back configuration for regenerative applications. Flying capacitor multilevel converters is used in high switching frequency high-bandwidth applications such as medium-voltage drives. Finally, cascaded H-bridge multilevel converters have been applied in high power and power quality for example, static synchronous compensators active filter and reactive power compensation applications, photovoltaic power conversion, magnetic resonance imaging, and uninterruptible power supplies. And also one of the growing applications for multilevel motor drives is electric and hybrid power trains.

For increasing voltage levels the number of switches also increases. Hence the switching losses and voltage stresses will increase and the circuit will become complex.
II. PROPOSED CASCADED MULTILEVEL INVERTER

A. Introduction

A cascaded multilevel inverter made up of series connected single full bridge inverter, each with their own isolated dc bus. The multilevel inverter can generate almost sinusoidal voltage waveform from several separate dc sources, obtained from solar cells, fuel cells, battery. A cascaded multilevel inverter made up of series connected single full bridge inverter, which has its own isolated dc bus. This multilevel inverter can generate nearly sinusoidal waveform voltage from several separate dc sources, obtained from fuel cells, batteries, solar cells, ultra capacitors, etc. This converter does not need any transformer or clamping diodes or flying capacitors.

Each level can generate five different voltage outputs $+2V_{dc}$, $+V_{dc}$, $0$, $-2V_{dc}$, and $-V_{dc}$ by connecting the dc sources to the ac output side by different combinations of the four switches. The output voltage of an Multilevel inverter is the sum of all the individual inverter outputs. Each of the H-Bridge’s switches only at the fundamental frequency, and each H-bridge unit produces a quasi- square waveform by phase-shifting its positive and negative phase legs switching time. Further, each switching device always conducts for 180° (or half cycle) regardless of the pulse width of the quasi-square wave so that this switching method results in equalizing the current stress in each active device.

This topology of inverter is suitable for high voltage and high power inversion because of its ability of synthesize waveforms with better harmonic spectrum and low switching frequency. Considering the simplicity and advantages, Cascaded H-bridge topology is selected for the presented work. A multilevel inverter has four advantages over the conventional bipolar inverter. Initially, the voltage stress on each switch is decreased due to series connection of the switches. Therefore, the rated voltage and the total power of the inverter could be safely increased. Second, the rate of change of voltage (dv/dt) is decreased due to the lower voltage swing of each switching cycle. Then, harmonic distortion is reduced due to more output levels. Finally, lower acoustic noise and electromagnetic interference (EMI) is obtained. The Proposed H Bridge multilevel inverter is shown in Fig. 1.

![Fig. 1 Proposed H Bridge multilevel inverter](image-url)
1) Modes of Operation of Five Level Inverter:

TABLE I: Switching States of 5 Level H Bridge Inverter

<table>
<thead>
<tr>
<th>V_{load}</th>
<th>MSr</th>
<th>MSd</th>
<th>MS+</th>
<th>MS-</th>
<th>AS_{11}</th>
<th>AS_{12}</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>4V_{dc}</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>Fig. 2</td>
</tr>
<tr>
<td>2V_{dc}</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>Fig. 3</td>
</tr>
<tr>
<td>0</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>Fig. 4</td>
</tr>
<tr>
<td>0</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>Fig. 5</td>
</tr>
<tr>
<td>-2V_{dc}</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>Fig. 6</td>
</tr>
<tr>
<td>-4V_{dc}</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>Fig. 7</td>
</tr>
</tbody>
</table>

B. Capacitor voltage balancing issues

Since the H Bridge contains series of capacitors (number of capacitors depends on the number of levels required), balancing them is an important issue in the proposed inverter. This section describes how capacitor imbalances occur during switching operation of the proposed inverter and possible solutions to overcome the issues.

1) Capacitor Voltage Balancing in lower 5 Level Inverter: The expected five level output voltage waveform of the lower H bridge inverter with five switching states is as shown in Fig. 8. Modes of charging and discharging of the two capacitors (C1 and C2) are shown in Fig. 9 (Red color dotted line shows the charging state of the capacitor, blue color dashed line shows the discharging state of the capacitor). Charging
and discharging of two capacitors for five different switching states along with the time interval is detailed in table II.

TABLE II: Capacitor Charging Status during Each Switching States for Two DC Link Capacitors

<table>
<thead>
<tr>
<th>Switching State</th>
<th>MS1</th>
<th>MS2</th>
<th>MS3</th>
<th>MS4</th>
<th>AS11</th>
<th>AS12</th>
<th>Status of C1</th>
<th>Status of C2</th>
<th>Time Duration</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>NC</td>
<td>NC</td>
<td>2.6 ms</td>
</tr>
<tr>
<td>2</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>Charging</td>
<td>Discharging</td>
<td>2.84 ms</td>
</tr>
<tr>
<td>3</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>NC</td>
<td>NC</td>
<td>5.86 ms</td>
</tr>
<tr>
<td>4</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>Discharging</td>
<td>Charging</td>
<td>2.84 ms</td>
</tr>
<tr>
<td>5</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>NC</td>
<td>NC</td>
<td>5.86 ms</td>
</tr>
</tbody>
</table>

From table II it is clear that DC link capacitors are charging and discharging only during the switching state 2 and 4. The time duration of switching states 2 and 4 in a cycle is 2.84 milli seconds each (refer Fig. 8 and table II).

2) Capacitor Voltage Balancing in lower 7 Level Inverter: The expected seven level output voltage waveform of the lower H bridge inverter with seven switching states is as shown in Fig. 10. Modes of charging and discharging of the two capacitors (C1, C2 and C3) are shown in Fig. 10 and Fig. 11 (Red color dotted line shows the charging state of the capacitor, blue color dashed line shows the discharging state of the capacitor). Charging and discharging of the two capacitors for five different switching states along with the time interval is detailed in table III.
TABLE III
Capacitor Charging Status during Each Switching States for Three DC Link Capacitors

<table>
<thead>
<tr>
<th>Switching State</th>
<th>MS1</th>
<th>MS2</th>
<th>MS3</th>
<th>AS1</th>
<th>AS2</th>
<th>AS3</th>
<th>Status of Capacitors</th>
<th>Time Duration</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF OFF OFF OFF OFF</td>
<td>1.84 ms</td>
</tr>
<tr>
<td>2</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF ON OFF ON OFF</td>
<td>1.82 ms</td>
</tr>
<tr>
<td>3</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF OFF OFF OFF OFF</td>
<td>2.16 ms</td>
</tr>
<tr>
<td>4</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF OFF OFF OFF OFF</td>
<td>4.0 ms</td>
</tr>
<tr>
<td>5</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF OFF OFF OFF OFF</td>
<td>1.82 ms</td>
</tr>
<tr>
<td>6</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF OFF OFF OFF OFF</td>
<td>2.16 ms</td>
</tr>
<tr>
<td>7</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF OFF OFF OFF OFF</td>
<td>4.0 ms</td>
</tr>
<tr>
<td>NC = No Change</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>Total: 30 ms</td>
</tr>
</tbody>
</table>

During switching state 2, Capacitors C1 and C2 are in charging state (red dotted line) and capacitors C3 is in discharging (blue dashed line) mode (Fig. 11(a)). The duration of charging and discharging are given in Table III.

Similarly during switching state 3, capacitor $C_1$ charges whereas capacitors $C_2$ and $C_3$ discharges as shown in Fig. 11(b). The duration of charging and discharging of capacitors are detailed in TABLE III.

![Fig. 12(a)](image1)

![Fig. 12(b)](image2)

**Fig. 12** Charging and discharging of capacitors $C_1$, $C_2$ and $C_3$ (a) During switching state 5 (b) During switching state 6

During switching state 5, capacitor $C_1$ discharges whereas capacitor $C_2$ and $C_3$ is in charging mode (Fig. 12(a)). Similarly during switching state 6, $C_1$ and $C_2$ discharge whereas $C_3$ charges (Fig. 12(b)). Duration of charging of all the three capacitors is detailed in TABLE III.

From TABLE III, the total charging and discharging time of capacitor $C_1$ and $C_3$ is 4.18 milli seconds, whereas the total charging time of capacitor $C_2$ is 3.84 milli seconds and discharging time of capacitor $C_2$ is 4.52 milli seconds. Thus over a cycle (for 50 Hz, 20 milli seconds), the net voltage in capacitor $C_2$ decreases, whereas charge on $C_1$ and $C_3$ is balanced. Hence capacitor balancing algorithm is needed in the case of seven-level inverter.

**III. BALANCING CAPACITOR VOLTAGE USING MULTILEVEL INVERTER**

In order to solve the capacitor voltage balancing issues in seven-level inverter, one has to reduce the discharging time of the capacitor $C_2$, so that the net voltage in capacitor over a cycle is positive. This should be done during switching states, 3 and 6, where the $C_2$ voltage decreases. Hence, a modified switching topology is proposed to increase the voltage across $C_2$. Fig. 13 shows the proposed modified switching topology.
It can be noticed in Fig. 13 that the proposed inverter voltage is allowed to switch between two levels during switching states 3 and 5. During switching state 3, the inverter voltage is switched between $2V_{dc}$ and $4V_{dc}$ for half of the duration and between $4V_{dc}$ and $6V_{dc}$ during next half duration. Thus reducing the duration of the switching state 3 in $4V_{dc}$ level where capacitor $C_2$ discharges. By doing this most of the time in switching state 3, proposed inverter voltage will be either in $2V_{dc}$ level or $6V_{dc}$ level, which increases the charging time of $C_2$. Fig. 14 shows the voltage waveforms of the modified switching topology of upper, lower and load voltage waveforms.

The load voltage waveform is derived by instantaneously adding the lower and upper inverter voltages. It can be further observed in Fig. 14 (zoomed Fig inside) that during switching state 3 of the lower inverter, the upper inverter should switch in the opposite manner to that of lower inverter. This is very important in order to make the load voltage to switch between $4V_{dc}$ and $5V_{dc}$, and also between $5V_{dc}$ and $6V_{dc}$. TABLE IV gives the switching states of the proposed inverter when it is driven from modified switching topology.

Fig. 16 illustrates the generation of switching signals for the upper and lower inverter. Signal $MR_{01}$ is the modified reference signal which is used to generate switching signals for switches $MS_1$ and $MS_4$, and modified reference signal $MR_{02}$ is used to generate switching signals for switches $MS_3$ and $MS_4$. Switching signals for the lower inverter is also given in 16.
The highlighted portions in the Table IV indicate that both the inverters (upper and lower) are switched at high frequencies but in the opposite manner i.e. when upper inverter voltage oscillates between zero and $-V_{dc0}$, the lower inverter voltage should be oscillating between $4V_{dc0}$ and $6V_{dc0}$ so that the net voltage across the load will be between $4V_{dc0}$ and $5V_{dc0}$. Further when the proposed inverter is driven from modified switching topology, the $C_2$ will be charging more than that of $C_1$ and $C_3$. Hence, the voltage across $C_2$ has to be sensed, and based on its instantaneous value either the generalized simplified switching algorithm or the modified modulation strategy has to be used.

**TABLE IV**: Switching States of Modified Modulation Strategy for Fifteen Level Inverter
IV. Simulation Results and Discussions

To validate the proposed inverter topology, simulations are carried out for the proposed inverter in Matlab/Simulink (Fig. 17). The generalized PWM modulation technique is implemented in the simulations up to 15 levels and it can be extended to any required level. The conditions for simulation and experiment are same. The simulation results of the 11 level and 15 level inverter is shown in Fig. 18 & 19.


V. CONCLUSION
The cascaded h bridge inverter is modeled and simulated using Matlab / Simulink. The capacitor voltage balancing issue is investigated in the simulated inverter. An algorithm is written to eliminate the capacitor voltage problem occurred in the inverter. The inverter is simulated using the modified switching algorithm in which the capacitor voltages are balanced. The capacitor voltages are compared with the conventional inverter. Due to this process the efficiency of the inverter is increased, losses are reduced and harmonics are reduced.

VI. FUTURE WORK
An inverter is modeled and simulated using the modified switching algorithm to balance the capacitor voltages using two antiparallel connected bidirectional switch. In future simulated model will be implemented as hardware.

REFERENCES


“Hossein Sepahvand, Student Member, IEEE, Jingsheng Liao, Member, IEEE, Mehdi Ferdowsi, Member, IEEE, and Keith A. Corzine, Senior Member, IEEE” Capacitor Voltage Regulation in Single-DC-Source Cascaded H-Bridge Multilevel Converters Using Phase-Shift Modulation
