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LOW POWER FPGA SOLUTION FOR BOTH DAB/DAB+ AUDIO DECODER

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ABSTRACT

A new progress to intend a DAB and DAB+ audio decoder is introduced to build up the quality of audio at the receiver end. Integrate an MPEG-1 Layer III (MP2) decoder and Advanced Audio Coding Low Complexity (AAC LC) decoder provides basic audio decoding for DAB and DAB+ in FPGA. The audio frames data are produce from DAB and DAB+ channel decoder are store in RAM. The bit stream de multiplexer parses the quantized spectrum data in the audio frame and provisions them in to the acoustic RAM. The converse quantization block reads the quantized spectra from the audio RAM, performs the inverse quantization computation, and writes reverse the consequence to the audio RAM. To put into practice a delta sigma demodulator to get better the SNR ratio. In order to decode both MP2 and AAC LC Decoder share the channel decoder and can share the same audio decoder. It simple methods improve high frequencies and stereo quality instead of complicated spectrum band replication and parametric stereo.The proposed decoder consumes low power.

Keywords: *Advanced audio coding, FPGA (Field Programmable gate array), chip design, Digital audio broadcasting.*

I. INTRODUTION

The quick improvement of digital communication for the period of the past decade has opened common Opportunities multimedia services, some of them working below rigorous limitations concerning the available bit rate for instead of audio contented. These include earthly and Satellite-based digital audio broadcasting and wireless music downloads to cellular phone since these applications cannot be served well using benchmark AAC, a superior audio format is chosen. That can deliver high audio class and full audio bandwidth still at very low data rates, for example at rates of 24 kb/s and lower than per audio channel.

To assist audio and music relief for very low bit rate As a frequent restriction, previous general audio coders usually have to reduce the transmitted Audio bandwidth when payment at low bitrates in order to stay away from surplus to requirements coding artefacts from being introduced in the transmitted low frequency section. HE-AAC technology was planned to overcome this difficulty by reproducing a wide audio Bandwidth independently of the coding bit rate by using audio bandwidth increase.

An improved description of the coder (AAC LC) is considered to additionally develop models of spatial discernment to accomplish an additional advancement in coding efficiency. In both cases, an additional objective was to attain this goal by resources of simple extensions to the reachable AAC architecture that come at a incomplete increase in computational difficulty.

The input samples are map into a sub sampled anxious demonstration using an examination filter bank. Using a perceptual model the signal Õs frequency and time dependent masking threshold is conventional. This gives the greatest coding error that can be introduced into the audio signal while still maintain perceptually unimpaired signal reputation.

This paper is organised as follows in section II both metrics and demerits of HE ACC V2 in DAB+ are analyzed. In section III DAB&DAB+ compactable Structure in proposed chip design is reported .In section IV , test result from the chip are
Presented and analyzed .Conclusion is stated in section.

II. ANALYSIS

In [1] presents a systematic examination of the modified discrete cosine transform/inverse modified discrete cosine transform (MDCT/IMDCT) algorithm by means of a matrix design. This approach consequence in innovative approving of the MDCT/IMDCT, enables the improvement of new algorithms, and makes lucid the organization between the algorithms.

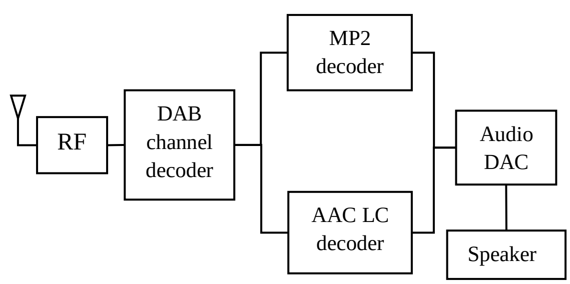
In [2] presents the modernized description of DAB (Digital Audio Broadcasting), i.e. DAB+, thus adopts HE-AAC as the new audio coding standard to amplify the spectrum efficiency and the forcefulness of the release audio quality. The DAB+ receivers at the present advancement to be small sized and convenient, thus strongly need low power consumption AAC decoder for maximum battery time.

In [3] presents An SOC based HW/SW co-design structural design for multi-standard audio decoding. A VLSI reconfigurable bypass through a filter bank based on CORDIC algorithm is developed to accelerate the multi standard decoding method. The proposed decoder is proposed to work on an SOC raise area, in which a RISC processor bears some decoding profession.

In [4] presents Perceptual audio coding has grown to be an necessary key technology for many types of multimedia services. A brief introduction into a number of issues as they occur in today's low bit speed audio coders. The approach is aggravated by the precision that, in spite the sophisticated state of today Õs perceptual audio coders, the managing of passing and pitched input signals still presents a most important tackle.

In [5] name MPEG-4 High-Efficiency AAC (HE-AAC) refers to a people of topical audio coders that were developed by the ISO/IEC Moving Picture Experts Group (MPEG) by consequential addition of the standard Advanced Audio Coding (AAC) architecture. These algorithmic extensions make possible a substantial augment in coding good organization relative to previous principles and other known systems.

DAB and DAB+ can share the similar channel decoder but cannot share the audio decoder because HE AAC V2 is not is not backward companionable with MP2. So in order to decode both DAB and DAB+ signals, the receiver must have MP2 and AAC LC audio decoders, as shown in Fig. 1.



RECEIVER

Fig.1. DAB/DAB+ Receiver structure

III.OVERVIEW OF AUDIO DECODING PROCESS

The main theme of paper is to add the MP2 decoder to the DAB baseband decoder without considerably increasing the silicon area and power use. The, AAC LC and MP2 decoders do not work at the same time, so we can share the circuitry. To reduce the hardware cost if we can find essential connection between the two decoders. This is possible because the two audio codec methods are all

Moving Pictures Experts Group(MPEG) and they have a similar decoding procedure.It can be seen that both decoders have the similar block bit stream De-multiplexer, inverse quantization, synthesis filter.

The AAC LC decoder is then designed as shown in Fig 4 to make it a similar structure to the proposed MP4 decoder. The gray blocks are the specific blocks of the AAC LC decoder. Other blocks can be shared with the MP2 decoder. For each block, it always reads data from the "audio_ram" and writes the results back to a different area of the same RAM, just as the MP2 decoder.

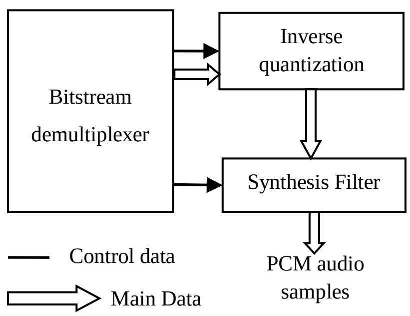


Fig.2. Common MP2 decoder procedure

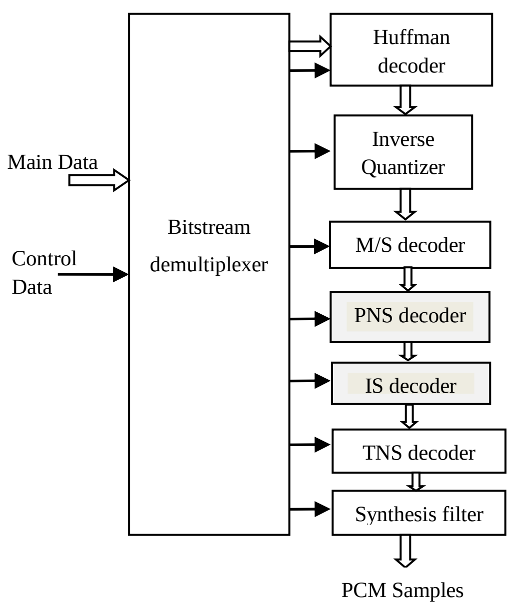


Fig.3. Common AAC LC decoder

A.ARCHITECTURE OPTIMIZATION

The bit pay load function is to read the data from the RAM. The bit stream Demultiplexer used to extracts the audio frame signals and decoding information. The inverse quantization block used reads the quantized spectra from the acoustic RAM, performs the inverse quantization computations, and writes back the consequence to the audio RAM. The inverse quantization performs as,

$$x_{rescale} = sign(x\_quant) * |x\_quant|^{\frac{4}{3}} * 2^{0.25(sf-SF\_OFFSET)} \quad sign(x\_quant) = \begin{cases} 1, x\_quant \geq 0 \\ -1, x\_quant < 0 \end{cases}$$

Reads the contrary quantized spectra from the audio RAM, generates the time area Pulse Code Modulation samples, and writes them backside to the audio RAM. The PCM samples are then understand writing out by the Digital Audio Interface to constrain an audio Digital-to-Analog Converter to play the sound.

In Huffman decoding, present are 12 Huffman codebooks. Eleven codebooks are used for range coding and one for scale-factor coding. There are two stages in ghostly Huffman decoding. Phase 1 is the Huffman decoding which unpacks the Huffman code lecture to list. Stage 2 is the regrouping of 2 or 4-tuples of signed or undetermined code language into quantized shadowy coefficients. Alongside with the 11 supernatural Huffman codebooks reserve 11 is a unique case.

It permits the encoding of quantized phantom coefficients even when their most important absolute value is better than 15.If the decoded value generation 16, an escape flag is used to signal the attendance of a so called escape progression. The runaway sequence consists of a run off prefix of N-bits 1, an escape partition of 1-bit 0, and and get away word of N+4 bits. The actual decoded values of the break away from chain are and break out words. Because the input utmost value of opposite quantization is 8191, the greatest length of the getaway sequence is 21 bits.

The inverse quantization block performs opposing quantization of decoding data. The **M/S** and consciousness stereo equipment make growth and add the redundancies uninvolved from the encoder to the rate of reappearance domain. M/S decoding, the left and right channel signals are dematrixed by either the identity matrix or the inverse M/S matrix. When the identity matrix is used, no computation is necessary. The **intensity stereo decoder** reconstructs the right channel spectrum from left channel spectrum and additional data.

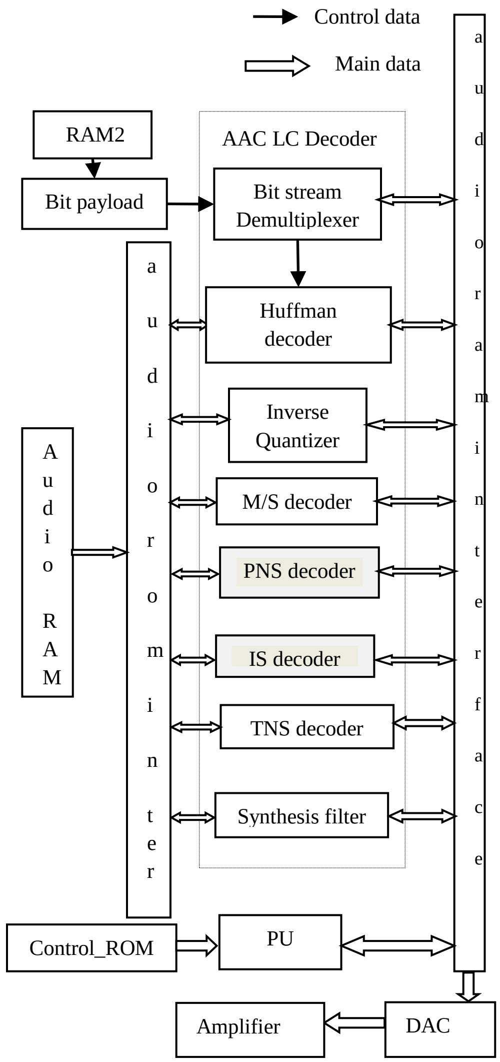


Fig.3. Proposed AAC LC decoder

The **Temporal Noise Shaping** move toward is based on two major considerations, Deliberation of the time/frequency duality between supernatural covering and (squared) Hilbert sachet and determining of quantization noise spectrum by means of open-loop extrapolative coding. Finally the **Perceptual Noise Substitution (PNS**) tool generates a set of random numbers to fill silent Samples with white noise audio and requires more complex calculation hardware than all previous Spectral Tools. The modified discrete cosine transform/inverse modified discrete cosine transform (MDCT/IMDCT) is used to realize the analysis/synthesis filter bank of time-domain aliasing cancellation scheme for sub band coding.

$$\bar{x}(n) = \sum_{k=0}^{N/2-1} X(k)\cos\left[\frac{\Pi}{2N}\left(2n+1+\frac{N}{2}\right)(2k+1)\right]$$

n=0, 1….N-1

Block	Complexity Ratio	Operation
Bit stream parser Huffman decoding	33.9	Decision
IQ	2.1%	Table look up, ADD
M/S	1.1%	ADD
IS	1.1%	MUL, ADD
TNS	10.6%	MUL
PNS		MUL
Filter bank	49.6%	MUL, ADD

TABLE 1- Characteristic and Operational Analysis of the decoding flow

B. SHARED MEMORIES

Many blocks of the MP2 and AAC LC decoder need to be optimized to reduce the computation and complexity. The detailed optimizations of these blocks are beyond the scope of this paper. The coefficients and constants desirable for each block are stored in the audio ROM. A very crammed and fully customized circuit which is self-possessed of adders, D-type flip-flops, and multipliers, and is designed especially for MP2 and AAC LC decoding. The PU and each block of the audio decoder swap data via the audio RAM boundary. The results from each block are written to the audio RAM, and then read out by PU for dispensation. After the PU has over processing, the results are written back to the audio RAM and wait to be read out by a supplementary block. It converts the PCM samples into audio indication.

TABLE 2-Number of Operation Cycles and Memory Accesses In Each Block

Block	Operating Cycle	Memory accesses
Bit stream Parsing	255×2	0
IQ	1024×2	Read :1024×2
Huffman decoder	1536×2	0
IS	1024	Read:1024 Write:1024
PNS		Read: Write:
Filter bank	15362×2	Read:21504×2 Write:12288×2

C. LOW POWER DESIGN

Two main methods are employed to reduce power consumption. The first method is algorithm design, together with circuit optimizations of each block of the MP2 and AAC decoders as described above.

Reducing the quantity of computations means the limit clock frequency of the decoder can be lowered, and as a result, the power expenditure reduces. The MP2 and AAC decoders will never work at the similar time, only one decoder will be in the energetic state and the other one can be totally close down, to save the power. Also for every audio decoder not all the blocks employment at the same time. So when some blocks of the audio decoder are dynamic, other blocks that are not active can be shut down to decrease the power disbursement when the inverse quantization block of the AAC decoder is active. The clocks of the sequential noise influential decoder, perceptual Noise changeover decoder, concentration stereo decoder, mid/side stereo decoder, and mixture filter can all be close down to keep power.

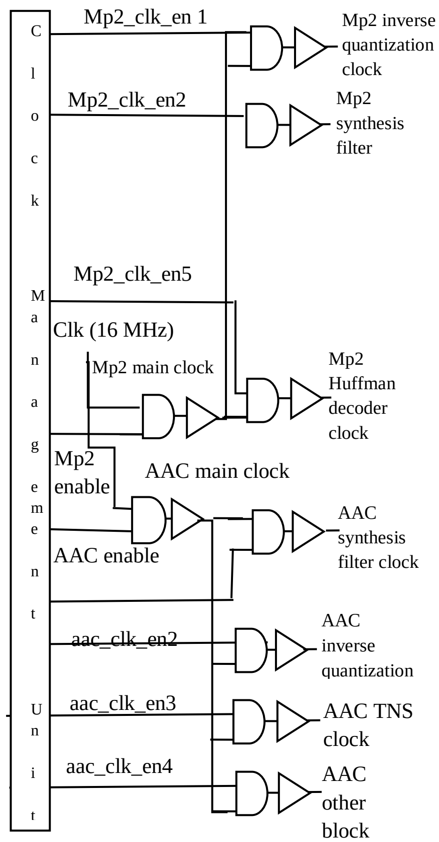


Fig.4.Proposed decoder clocking network.

The controls of all the clocks are managed by the clock supervise unit in the audio decoder. If MP2 state is enable at that time above all MP2 task are enable state. If AAC state is enable at that time above all AAC task are enable state. Same time maintaining the high audio quality.

D. ACHIEVING HIGH FREQUENCY AND STEREO

The algorithm of SBR and PS is much more complex than that of the AAC LC decoder itself. The computations of SBR and PS are about 1.6 and 1.4 times as much as the AAC LC decoder, whereas their improvements to coding efficiency are only about 24% and 33% , respectively.

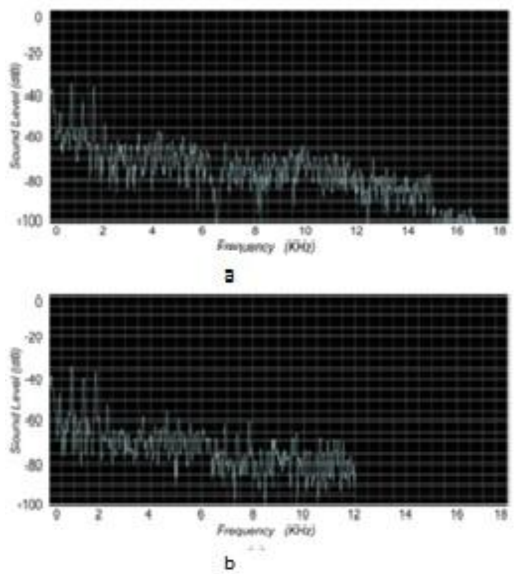
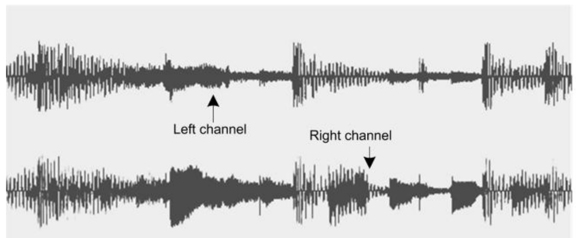


Fig.5. a. Output using the standard SBR decoder. b.Output from the proposed decoder

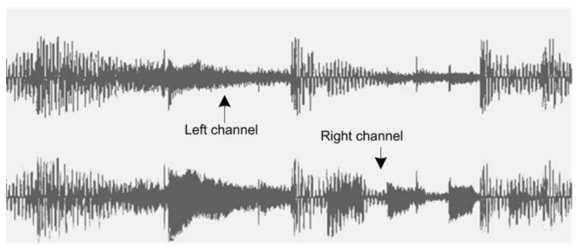
The audio data processed by AAC LC decoder can be described in IMDCT domain as $X1(f) = \text{sum}(ai * f1(i))$,where $i = 0, 1, \ldots 1023$, $f1(i)$ is the spectral line in the IMDCT domain, and a is the coefficient. Retransformed to SBR's frequency domain using an analysis quadrature mirror filter (QMF). The spectrum of SBR has lower frequency resolution but higher time resolution than the AAC spectrum. So $x1(t)$ becomes to $X2(b, l)$, where b is the SBR band index, ranging from 0 to 31, and l is the time index, also ranging from 0 to 31. SBR then generates and adjusts the high-frequency components ($X2(b, l)$ with $32 \leq b < 64$) with a set of complicated algorithms. Finally, SBR transforms $X2(b, l)$ (after b is expanded to 63) back into the time domain (marked as $x_2(t)$ with a synthesis QMF filter, at a doubled sample rate. $x_2(t)$ and $x1(t)$ correspond to the same audio, but

$x2(t)$ has high-frequency components whereas $x1(t)$ has none. Because $x2(t)$ and $x1(t)$ have strong relationships, we considered finding a relationship between their spectra $X1(f)$and $X2(b, l)$, so that the complex computations in the QMF domain can be performed in the IMDCT domain directly. In this design, this relationship is simply $f = 32 \times b+l$.

The standard PS decoder operates on the same spectrum as SBR, with further processes applied to the lower frequency bands. In this way, the PS decoder complexity can be greatly reduced while still keeping most of the stereo effects of the standard method. Because SBR and PS filters are not the presented AAC LC decoder will still work at half the sample frequency of 24 and 16 kHz, instead of 48 and 32 kHz. Fig. 6 compares the spectra generated by the standard SBR method with those of the simple method presented above for a 64-kb/s AAC+ test vector (48 kHz sampling frequency).



(a)



(b)

Fig.6.

a. output using the standard PS decoder.

b. output from the proposed decoder.

The original audio has frequencies only between 0and 7 kHz, as shown in Fig. 6(a). The standard SBR decoder can expand the spectrum to 17 kHz, as shown in Fig. 6(b). The presented method can only expand the spectrum to 12 kHz, as shown in Fig. 6(c). However, within 7–12 kHz, the spectrum amplitudes of the simple method are very close to those of the standard method. So the simple method will reproduce most of the high-frequency components, thus improving the audio quality

IV.IMPLEMETATON RESULT

A.Audio Decoding Performance Test

Prototype receivers based on the fabricated chip were designed. The laboratory tests and field tests were carried out. Over 300 DAB and DAB programs recorded from the U.K.,France, Germany, Korea, and Australia were used for testing and the results analyzed.

B.Audio Quality of the DAB and AAC LC DAB+ Programs

For DAB and AAC LC DAB+ programs (no SBR and PS applied), the audio quality can be measured objectively by the ISO/IEC 13818-4 compliance test which uses the root mean square (rms) of the differences between the output of the decoder under test (DUT) and the reference decoder, as defined in the following equation,

$$rms = \left({}^{1}/_{N} \sum_{n=0}^{N-1} \left(out(n) - ref(n)\right)\right)$$

Where N is the total number of samples under test, out (n) denotes the output sample of the DUT, and ref (n) denotes the output sample of the reference decoder. In our test, the reference decoder is a high-accuracy floating-point decoder implemented in Xilinx ISO/IEC 13818-4 defines two classes of audio decoders: full-accuracy and limited-accuracy ones. Their requirements, together with the test results of the presented audio decoder, are listed in table It can be seen that our design is better.

DECODING PERFORMANCE TEST RESULT OF THE AACLC DAB+ PROGRAMS

	MP2 rms	**MP2 max diff**	**AAC rms**	**AAC Max diff**
Full accuracy	**<8.8×10**	**6.1×10**	**<8.8×10**	**6.1×10**
Limited accuracy	**<1.4×10**	**–**		**–**
Our design	**<1.2×10**	**8×10**	**1.5×10**	**2.0×10**

Than the “limited-accuracy” specification and close to the “full accuracy” specification. The test shows that our design can decode all the DAB programs and high bit rate DAB+ programs. For high bit rate DAB+ programs which do not use SBR and PS, our design based on AAC LC can achieve the expected high quality. This is very important because these programs are the highest quality programs so they are allocated high bit rates.

C.Design flow

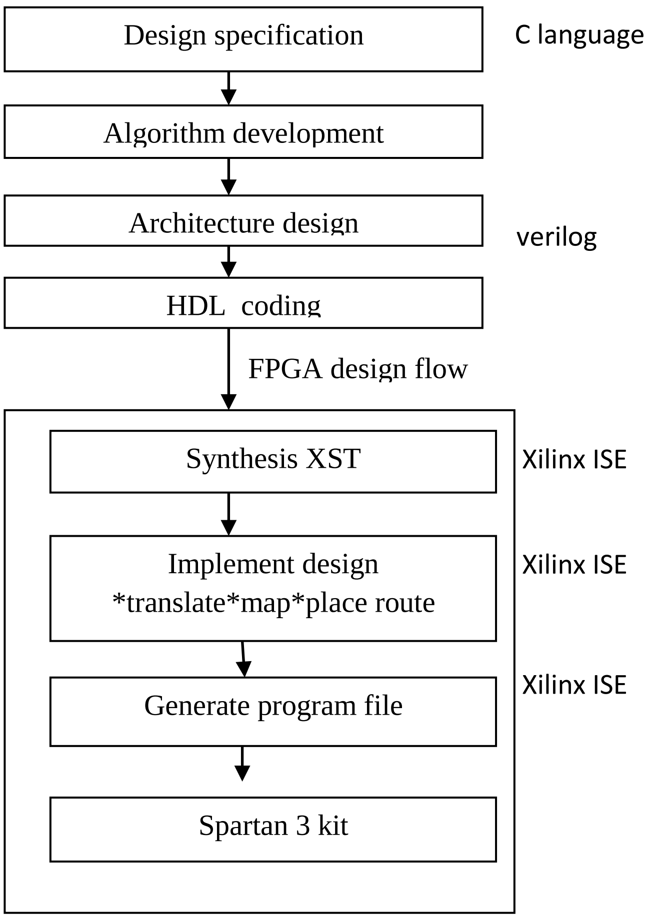


Fig.7. complete system level design flow

The Design flow in overall system in shown fig for a complete system design, the FPGA prototype is developed.

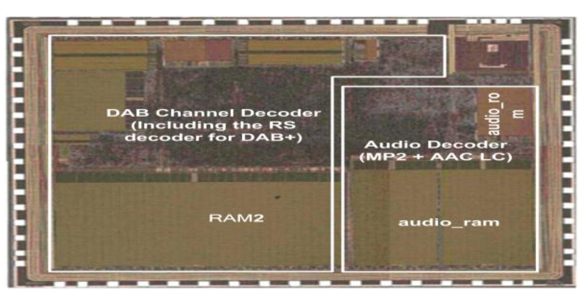


Fig.8.chip layout of the decoder.

V.CONCLUSION

AAC LC augmented spectrum effectiveness compared to MP2. SBR and PS have consequence on low bit rate programs but the slanted emotion of the effect is not dependable, and the upgrading is counteracted by other factors such as complication and higher power consumption for decoding. MP2 and AAC LC decoder are both based on the psychoacoustic model for audio compression using a time-to-frequency transformation. DAB and DAB+ should be tolerant and/or compatible to each other; to overcome the conflicts and the chaos of the two incompatible standards. To verify the designed system by using simulation. The result of simulation showed in both Xilinx ISE tool. Then the power consumption and area occupied by the architecture have been analyzed and at the same time maintaining the high audio quality.

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