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PERFORMANANCE ANALYSIS OF A 1-BIT FULL ADDER USING 45nm TECHNOLOGY

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ABSTRACT

Increased usage of battery operated portable devices demands VLSI and ultra large scale integration (ULSI) designs with an improved power delay characteristics. Full adder being one of the most fundamental building block of all the circuit applications. A 1-bit full adder design employing both complementary metal oxide semiconductor (CMOS) logic and transmission gate logic is designed. The circuit was implemented for a single bit using tanner tool in 45nm technology and the parameter such as power is compared with the existing designs of complementary pass transistor logic (CPL), transmission function adder (TFA), transmission gate adder (TGA), Hybrid pass logic with static CMOS output drive full adder (HPSC) and so on. For 45nm technology, the average power consumption was found to be extremely low resulting from the deliberate incorporation of very weak CMOS inverters coupled with the strong transmission gates. The same design can further extend for implementing 32 bit full adder also. The present implementation was found to offer significant improvement in terms of power.

Keywords: ***CMOS, TGA, CPL, HPSC, TFA***

I. INTRODUCTION

Wireless communication plays an important role in upgrading communication technology. The increased usage of the battery operated portable devices like cellular phones, personal digital assistants (PDAs) and notebooks demands supports wireless transmission and it requires VLSI and ultra large scale integration designs with a improved power delay characteristics. Full adder being one of the most fundamental building block of all the aforementioned circuit applications, remain a key focus domain of the researchers over the years. Different logic styles each having its own merits and demerits. The full-adder circuit adds three one-bit binary numbers (C A B) and outputs two one-bit binary numbers, a sum (S) and a carry (C1). The full-adder is usually a component in a cascade of adders, which add 8, 16, 32, etc. binary numbers. The carry input for the full-adder circuit is from the carry output from the circuit above itself in the cascade. The carry output from the full adder is fed to another full adder below itself in the cascade. The demand and popularity of the portable electronics is driving the designers towards smaller silicon area, lesser power consumption and lesser delay. Full Adders are basic blocks of many circuits, especially in Arithmetic operations performed by processors, compressors,
comparators, floating point unit and so on. There are many standard implementations in designing the Full Adder. Although the functionality is same, the way of producing the intermediate nodes and transistor count is varied. In different logic styles, one performance aspect is achieved at the cost of others. Small area and high performance are two conflicting constraints. The power consumed for any given function in CMOS circuit must be reduced for either of the two different reasons: One of these reasons is to reduce heat dissipation in order to allow a large density of functions to be incorporated on an IC chip. Any amount of power dissipation is worthwhile as long as it doesn't degrade overall circuit performance. The other reason is to save energy in battery operated instruments same as electronic watches where average power is in microwatts The logic style used basically influence the size, speed, wiring complexity and power dissipation. Circuit Size depends on the number of transistors, their sizes and on the wiring complexity. In the second section various styles of Full Adder using Majority Function and the proposed Full Adder cell is implemented. In the third section simulation results, layout of the Proposed Full Adder is provided and comparison of power consumption for different power supply voltages and Area for different implementations are provided. In conventional full adder circuits, we use CMOS technology i.e. PMOS and NMOS are used as a switch in complementary mode. Such applications of NMOS and PMOS as a switch is called pass transistor logic. In Transmission Gates, both NMOS and PMOS transistors are combined in parallel fashion. When performance of both the circuits was compared, transmission gate circuit consumed less power as compared to the pass transistor circuit designed using CMOS logic. In electronics, pass transistor logic (PTL) describes several logic families used

in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Pass transistor logic often uses fewer transistors, runs faster, and requires less power than the same function implemented with the same transistors in fully complementary CMOS logic. In conventional logic families input is applied to gate terminal of transistor but in PTL it is also applied to source/drain terminal. When used as pass transistor, the device may conduct current in either direction. The demand and popularity of the portable electronics is driving the designers towards smaller silicon area, lesser power consumption and lesser delay. Full Adders are basic blocks of many circuits, especially in Arithmetic operations performed by processors, compressors, comparators, floating point unit and so on. There are many standard implementations in designing the Full Adder. Although the functionality is same, the way of producing the intermediate nodes and transistor count is varied. In different logic styles, one performance aspect is achieved at the cost of others. Small area and high performance are two conflicting constraints. The power consumed for any given function in CMOS circuit must be reduced for either of the two different reasons: One of these reasons is to reduce heat dissipation in order to allow a large density of functions to be incorporated on an IC chip. Any amount of power dissipation is worthwhile as long as it doesn't degrade overall circuit performance. The other reason is to save energy in battery operated instruments same as electronic watches where average power is in microwatts.

II. DESIGN APPROACH

The full adder circuit is represented by three blocks. Module 1 and Module 2 are the XNOR modules that generate the sum signal (SUM) and module 3 generates the output carry signal (C_{out}). Each module is designed individually such that the entire adder circuit is optimized in terms of power, delay and area. These modules are discussed below in detail.

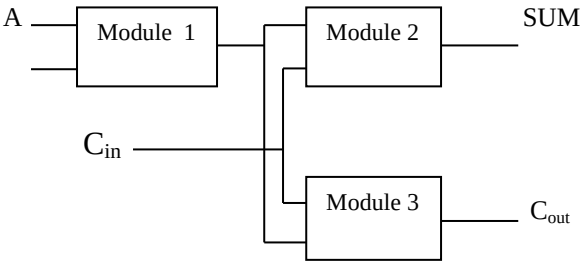

Figure 1 Schematic Structure of a Full Adder

A. Modified xnor module

In the given full adder circuit, XNOR module is responsible for most of the power consumption of the entire adder circuit. Therefore this module is designed to minimize the power to the best possible extend with avoiding the voltage degradation possibility. The modified XNOR circuit where the power consumption is reduced significantly by deliberate use of weak inverter (channel width of transistor being small) formed by transistor Mp1 and M1. Full swing of the levels of output signals is guaranteed by level restoring transistors Mp3 and Mn3. Various XOR/ XNOR topologies have already been reported. The XOR/ XNOR reported uses four transistors but at the cost of low logic swing. To the contrary, the XOR/ XNOR used six transistors to get better logic swing compared with that of 4T XOR/ XNOR. In this paper also, the XNOR module employed 6T, but having different transistor arrangement than that of 6T XOR/ XNOR.

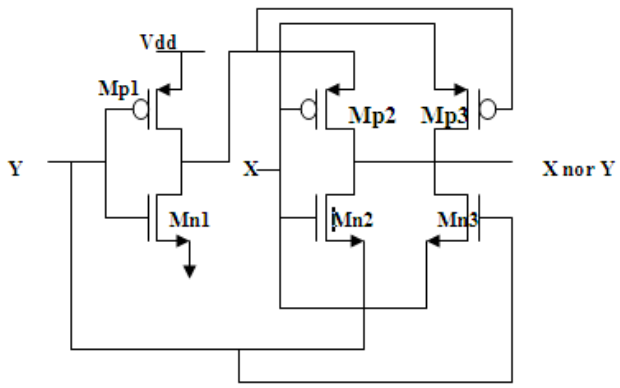

Figure 2 Xnor Module

B. Carry generation module

In the circuit, the output carry signal is implemented by the transistors Mp7, Mp8, Mn7 and Mn8 are shown. The input carry signal (Cin) propagates only through a single transmission gate (Mn7 and Mp7) reducing the overall carry propagation path significantly. The deliberate use of strong transmission gates (channel width of transistors Mn7, Mp7, Mn8 and Mp8 is made large) guaranteed further reduction in propagation delay of the carry signal.

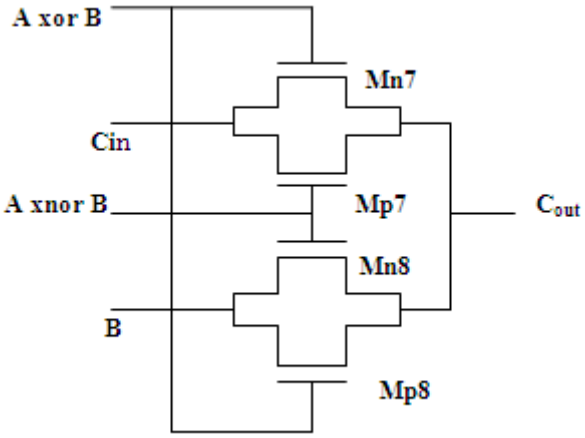

Figure 3 Carry Generation Module

III. OPERATION OF FULL ADDER

The detail diagram of the proposed full adder is given below. The sum output of the full adder is implemented by XNOR modules. The inverter comprised of transistors Mp1 and Mn1 generate B which is effectively used to design the controlled inverter using the transistor pair Mp2 and Mn2. Output of this controlled inverter is basically the XNOR of A and B. But it has some voltage degradation problem which has been removed usig two pass transistors Mp3 and Mn3. PMOS transistors (Mp4, Mp5 and Mp6) and nMOS transistors (Mn4, Mn5 and Mn6) realize the second stage XNOR module to implement the complete SUM fucntion. The condition for Cout generation has been deducted as follows:

If A=B then C_{out} = B; else C_{out}= C_{in}

The simulation of the full adder was carried out using 180nm technology and compared with the other potential adder designs reported [1]-[11] with special emphasis on design approach. The aim to optimize both power and delay of the circuit, the power-delay product (PDP) that is the energy consumption has been minimized in the proposed case. The power consumption could be minimized by mainly sizing the transistors in inverters circuits; while the carry propagation delay could be improved by mainly sizing the transistors of the transmission gates present between the paths from C_{in} to C_{out}.

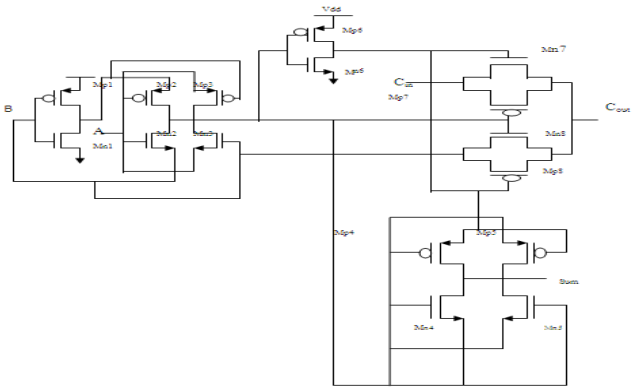

Figure 4 Circuit Diagram of Full Adder Using CMOS Inverter and Pass Transistor

The given hybrid adder requires only 16 transistors whereas the other hybrid adders require more than 20 transistors. The average power consumed by the proposed full adder is significantly lower than that of other hybrid full adders. The use of less number of transistors in this paper also improved the speed. Because of reduction in average power consumption and propagation delay, the PDP of the proposed hybrid full adder is significantly improved in comparison with the earlier hybrid adders. A single bit adder cell designed for optimum performance may not perform well under deployment to real time conditions. This is because when connected in cascaded form, the driver adder cell may not provide proper input signal level to the driven cells. The cumulative degradation may lead to faulty output and the circuit may malfunction under low supply voltages.

To analyze the success of the proposed full adder during its actual use in VLSI applications, provide a realistic environment, buffers are added at the input and the output of the test bench [13], [15]. The inputs to the adder cell, are fed through the buffers to incorporate the effect of input capacitance and the outputs are also loaded with buffers to ensure proper loading condition. The proposed full adder is simulated using several test bench setup. These test benches are having the common prototype of three buffers at the input and two buffers at the output. They only differed in the number of stages of adder cells used in between the input and output of the simulation setup. The number of stages varied starting from two and increased gradually. It was observed that the carry propagation delay from the input to the output started rising significantly in the order of two after the third stage. Therefore, the three-stage simulation test bench is selected for simulation purpose. Further, the behavior of performance parameters (power and delay) could be measured from the second adder cell by using this test bench. The logic style used basically influence the size, speed, wiring complexity and power dissipation. Circuit Size depends on the number of transistors, their sizes and on the wiring complexity. In the second section various styles of Full Adder using Majority Function and the proposed Full Adder cell is implemented. In the third section simulation results, layout of the Proposed Full Adder is provided and comparison of power consumption for different power supply voltages and Area for different implementations are provided.

In conventional full adder circuits, we use CMOS technology i.e. PMOS and NMOS are used as a switch in complementary mode. Such applications of NMOS and PMOS as a switch is called pass transistor logic. In Transmission Gates, both NMOS and PMOS transistors are combined in parallel fashion. When performance of both the circuits was compared, transmission gate circuit consumed less power as compared to the pass transistor circuit designed using CMOS logic. The full-adder circuit adds three one-bit binary numbers (C A B) and outputs two one-bit binary numbers, a sum (S) and a carry (C_{out}). The full-adder is usually a component in a cascade of adders, which add 8, 16, 32, etc. binary numbers. The carry input for the full-adder circuit is from the carry output from the circuit above itself in the cascade. The carry output from the full adder is fed to another full adder below itself in the cascade. In electronics, Pass Transistor Logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Pass transistor logic often uses fewer transistors, runs faster, and requires less power than the same function implemented with the same transistors in fully complementary CMOS logic. In conventional logic families input is applied to gate terminal of transistor but in PTL it is also applied to source/drain terminal. When used as pass transistor, the device may conduct current in either direction. A transmission gate is defined as an electronic element that will selectively block or pass a signal level from the input to the output. This solid-state switch is comprised of a PMOS transistor and NMOS transistor. When C = 1, X and Y are connected, both logic zero and logic one are passed without degradation. A transmission gate has three inputs, called source, n- gate, and p-gate; and it has one output, called drain. The two transistors, an NMOS and a PMOS are connected in parallel configuration. When the control input is a logic zero (negative power supply potential), the gate of the NMOS is also at a negative supply voltage potential. The transmission gate consists of two MOSFETs, one n-channel responsible for correct transmission of logic zeros, and one p-channel, responsible for correct transmission of logic ones.

The gate terminal of the PMOS is caused by the inverter, to the positive supply voltage potential. Regardless of on which switching terminal of the transmission gate (X or Y) a voltage is applied, the gate-source voltage of the NMOS is always negative, and the PMOS is always positive. Accordingly, neither of the two transistors will conduct and the transmission gate turns off. When the control input is a logic one, so the gate terminal of the NMOS is located at a positive supply voltage potential. By the inverter, the gate terminal of the PMOS is now at a negative supply voltage potential. As the substrate terminal of the transistors is not connected to the source terminal, the drain and source terminals are almost equal and the transistors start at a voltage difference between the gate terminal and one of these conducts. One of the switching terminals of the transmission gate is raised to a voltage near the negative supply voltage, a positive gate-source voltage (gate-to-drain voltage) will occur at the NMOS, and the transistor begins to conduct, and the transmission gate conducts. The voltage at one of the switching terminals of the transmission gate is now raised continuously up to the positive supply voltage potential, so the gate-source voltage is reduced (gate-drain voltage) on the NMOS, and this begins to turn off. At the same time, the PMOS has a negative gate-source voltage (gate-to-drain voltage) builds up, whereby this transistor starts to conduct and the transmission gate switches. Thereby it is achieved that the transmission gate passes over the entire voltage range. Transmission gates are used in order to realize electronic switches and analog multiplexers.

A .Calculation of Power Consumption

A full adder adds binary numbers and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as A, B, and C_{in}; A and Bare the operands, and C_{in} is a bit carried in from the previous less significant stage.The full adder is usually a component in a cascade of adders, which add 8, 16, 32, etc. bit binary numbers. The circuit produces a two-bit output, output carry and sum typically represented by the signals $C_{out}$and S where SUM = 2 X C_{out} + S. Power consumption of the hybrid full adder can be broadly classified into two categories: 1) static power and 2) dynamic and short-circuit power [13]–[15]. Static power, originated from biasing and leakage currents, in most of the CMOS-based implementations is fairly low when compared with its dynamic counterpart [3]. In order to minimize the static power further, the weak inverters having large channel width of 800/240 nm (in 180-nm technology) for Mp1 and Mp6, respectively, and 400/120 nm (180nm technology) for Mn1 and Mn6 respectively was incorporated deliberately [1]. The overall static power in 180-nm technology was found to be 2.139 nW which is very low when compared with the overall dynamic power (4.1563 μW) [1]. This increase in static power is possibly due to the increase in the subthreshold conduction current and gate leakage [3]. The dominant component of the power consumption, the dynamic power, arises because of charging and discharging of the load capacitances. The minimum power consumption of the proposed system for a power supply of 1.1v is given as 3.737162 μW. The load capacitance, C_{load}, can be expressed as a combination of a fixed capacitance, C_{fix}, and a variable capacitance, C_{var}, as follows:

$$C_{load} = C_{fix} + C_{var} . \quad (1)$$

In this expression, C_{fix} is the technology-dependent (principally originated from diffusion capacitance) and interconnect dependent capacitances. The interconnect dependent capacitance is minimized by efficient layout design in this case. On the other hand, C_{var} is composed of the input capacitances of subsequent stages and a part of the diffusion capacitance at the gate output and can therefore be taken care of by proper sizing of the transistors.

$$\text{Power} = VDD * f_c * \sum_{j=1}^{N} aj * Cloadj * \Delta Vj \quad (2)$$

It is clear from (2) that the transistor size could be an effective parameter for reducing dynamic power consumption. Also, the inverters have to be weak and the transmission gates have to be strong. Initially, the transistor sizes were chosen on the theoretical background of the design. Subsequently, they were varied (through simulations) in the vicinity of the previously set values to obtain the best performance in terms of power and delay. The optimized transistor sizes of the proposed full adder are already summarized in Table I. It was observed that the static power of the developed circuit varied from 56.38 to 392.4 pW for variation in supply voltage from 0.8 to 2.5V in 180-nm technology [1].

In contrast, the dynamic power varied from 114.08nW to 6.125μW for the same voltage variation. Considering the similar kind of implementation using 90-nm technology [1] with a voltage range of 0.6–1.5 V, the dynamic power consumption was found to be reduced dramatically while the static power consumption increased in comparison with the 180-nm case. It is worth mentioning here that at 180-nm technology, the threshold voltage is 0.7–0.8 V and the MOSFET break down takes place after 2.5 V. So voltage was varied from 0.8 to 2.5 V in 180-nm node. On the other hand, at 90-nm technology, the threshold voltage is 0.6 V and the MOSFET break down occurs at 1.5 V. So, the voltage was varied from 0.6 to 1.5 V in the 90-nm case.

TABLE I - SIMULATION RESULT FOR FULL ADDERS IN 45NM TECHNOLOGY WITH 1.1V POWER SUPPLY

Design	Average power (μW)	Transistor Count	References
CMOS	6.2199	28	4,15
Mirror	6.0797	28	15
CPL	7.7198	32	5,6
TFA	8.2491	16	14
TGA	8.4719	20	7,8
14 T	12.7217	14	10
10 T	14.3449	10	14
HPSC	6.3798	22	11
24 T	15.91	24	13
FA Hybrid	5.978	24	2
FA DPL	19.56	22	6

FA SR CPL	20.78	20	6
CMOS and Transmission Logic in 180nm	5.038266	16	1
Majority Based	6.3227	----	9
CMOS and Transmission Logic in 45nm	3.737159	16	Proposed

TABLE II . Transistor Size of Proposed Full Adder

Transistor Size	45nm Technology	
	Width(W) nm	Length(L) nm
Mn1, Mn6	400	45nm
Mp1,Mp6	800	45nm
Mn2,Mn3	400	45nm
Mp2,Mp3	800	45nm
Mn4,Mn5	400	45nm
Mp4,Mp5	800	45nm
Mn7,Mn8	400	45nm
Mp7,Mp8	800	45nm

The pass transistor is driven by a periodic clock signal and acts as an access switch to either charge up or charge down the parasitic capacitance C_x, depending on the input signal V_{in}. Thus, the two possible operations when the clock signal is active (CK = 1) are the logic "1" transfer (charging up the capacitance C_x to a logic-high level) and the logic "0" transfer (charging down the capacitance C_x to a logic-low level). In either case, the output of the depletion load NMOS inverter obviously assumes a logic- low or a logic-high level, depending upon the voltage V_x. Therefore, NMOS passes- a strong '0' and weak '1'. Similarly, it can be shown for PMOS that it passes- a strong '1' and weak '0'. With an aim to optimize both power and delay of the circuit, the power-delay product (PDP), that is, the energy consumption has been minimized in the proposed case. It was observed that in the present design, the power consumption could be minimized by mainly sizing the transistors in inverter circuits; while the carry propagation delay could be improved by mainly sizing the transistors of the transmission gates present between the paths from C_{in} to C_{out}. The transistor sizes of the proposed full adder circuit are given in Table I for both the technologies (90 and 180 nm) [1]. Power consumption, propagation delay, and PDP of the 180nm full adder along with that of existing full adders.[1]

IV RESULT

The circuit diagram of full adder with 45nm technology is designed using tanner tool version 13. The circuit with power supply of 1.1V is given as follows.

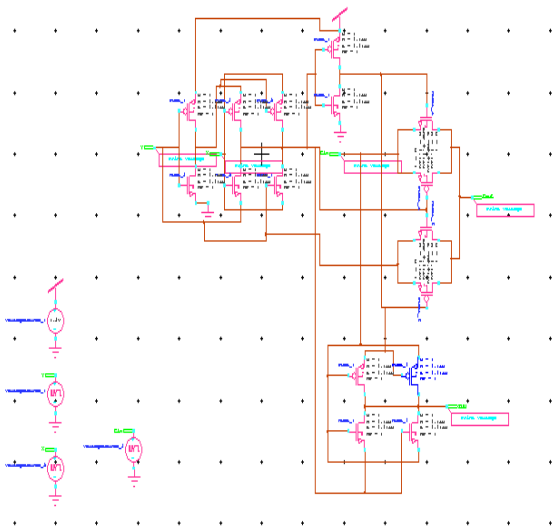

Figure 5 Circuit Diagram of a 1-bit Full Adder using Tanner Tool

The suggested method was developed and tested by using Tanner Tool with 45nm technology and compared with other standard design approaches like CMOS, CPL, TFA, TGA and other designs. The power consumption of the proposed 1-bit full adder is designed with the outcome of 3.737159μW. The simulation status shows the average power consumption is given above.

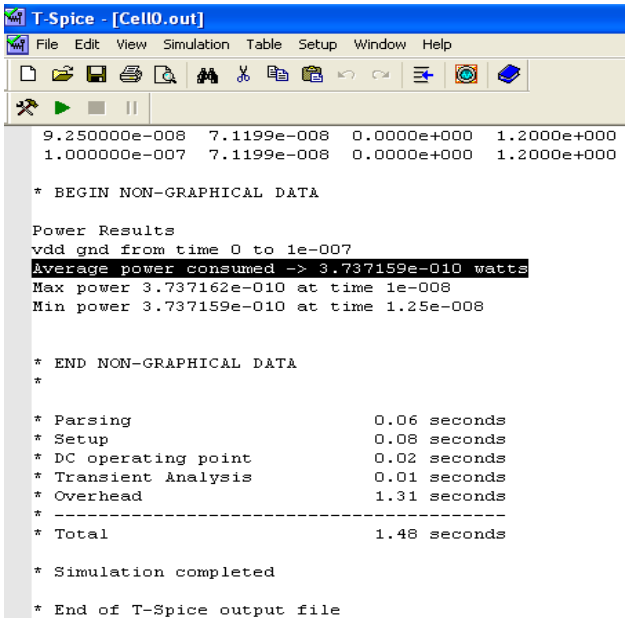

Figure 6 Simulation Status of a 1-bit Full Adder

The waveform representation of a 1-bit full adder is given where the inputs are X,Y,Z. According to the input, output will be displayed.

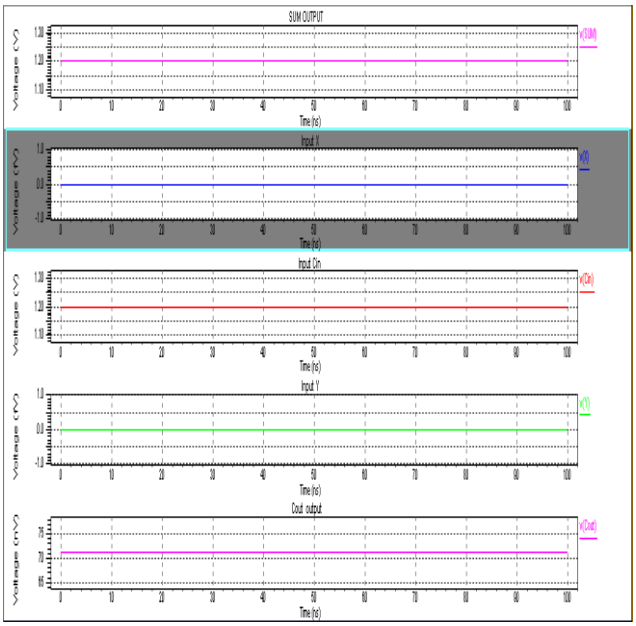

Figure 7 Output Waveform of a 1-bit Full Adder using 45nm Technology.

V CONCLUSION

In this paper a low power hybrid 1-bit full adder has been proposed. The simulation was carried out using Tanner tool in 45nm Technology with 1.1V of power supply and compared with other standard design. The power consumption of

the proposed full adder is reduced up to 3.737159μW. The efficient coupling of strong transmission gates driven by weak CMOS inverters lead to fast switching speeds excluding buffer.

REFERENCES

[1] C.-K. Tung, Y.-C. Hung, S.-H. Shieh, and G.-S. Huang, "A low-power high-speed hybrid CMOS full adder for embedded system," in *Proc. IEEE Conf. Design Diagnostics Electron. Circuits Syst.*, vol. 13. Apr. 2007, pp. 1–4.

[2] S. Goel, A. Kumar, and M. A. Bayoumi, "Design of robust, energyefficient full adders for deep-submicrometer design using hybrid-CMOS logic style," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 12, pp. 1309–1321, Dec. 2006.

[3] N. H. E. Weste, D. Harris, and A. Banerjee, *CMOS VLSI Design: A Circuits and Systems Perspective*, 3rd ed. Delhi, India: Pearson Education, 2006.

[4] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Delhi, India: Pearson Education, 2003.

[5] D. Radhakrishnan, "Low-voltage low-power CMOS full adder," *IEE Proc.-Circuits Devices Syst.*, vol. 148, no. 1, pp. 19–24, Feb. 2001.

[6] R. Zimmermann and W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," *IEEE J. Solid-State Circuits*, vol. 32, no. 7, pp. 1079–1090, Jul. 1997.

[7] C. H. Chang, J. M. Gu, and M. Zhang, "A review of 0.18-μm full adder performances for tree structured arithmetic circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 6, pp. 686–695, Jun. 2005.

[8] A. M. Shams, T. K. Darwish, and M. A. Bayoumi, "Performance analysis of low-power 1-bit CMOS full adder cells," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 10, no. 1, pp. 20–29, Feb. 2002.

[9] M. L. Aranda, R. Báez, and O. G. Diaz, "Hybrid adders for high-speed arithmetic circuits: A comparison," in *Proc. 7th IEEE Int. Conf. Elect. Eng. Comput. Sci. Autom. Control (CCE)*, Tuxtla Gutierrez, NM, USA, Sep. 2010, pp. 546–549.

[10] M. Vesterbacka, "A 14-transistor CMOS full adder with full voltageswing nodes," in *Proc. IEEE Workshop Signal Process. Syst. (SiPS)*, Taipei, Taiwan, Oct. 1999, pp. 713–722.

[11] M. Zhang, J. Gu, and C.-H. Chang, "A novel hybrid pass logic with static CMOS output drive full-adder cell," in *Proc. Int. Symp. Circuits Syst.*, May 2003, pp. 317–320.

[12] P. Prashanth and P. Swamy, "Architecture of adders based on speed, area and power dissipation," in *Proc. World Congr. Inf. Commun. Technol. (WICT)*, Dec. 2011, pp. 240–244.

[13] M. J. Zavarei, M. R. Baghbanmanesh, E. Kargaran, H. Nabovati, and A. Golmakani, "Design of new full adder cell using hybrid-CMOS logic style," in *Proc. 18th IEEE Int. Conf. Electron., Circuits Syst. (ICECS)*, Dec. 2011, pp. 451–454.

[14] I. Hassoune, D. Flandre, I. O'Connor, and J. Legat, "ULPFA: A new efficient design of a power-aware full adder," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 8, pp. 2066–2074, Aug. 2010.

[15] K. Navi, M. Maeen, V. Foroutan, S. Timarchi, and O. Kavehei, "A novel low-power full-adder cell for low voltage," *VLSI J. Integr.*, vol. 42, no. 4, pp. 457–467, Sep. 2009.