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Abstract - A new enhanced metal oxide semiconductor device called BE-LDMOS (BJT Enhanced Laterally Double diffused Metal Oxide Semiconductor) has been proposed which has improved performance in terms of reduced ON resistance and increased switching speed. ON resistance has been reduced by increasing the drain current for a gate voltage with the help of parasitic BJT. 26% reduction in ON resistance and 7.8% improvement in switching speed had been attained without affecting other performance parameters like off state breakdown voltage and transconductance (g_m).SOI (Silicon On Insulator) technology has been used with fabrication steps similar to that of LDMOS.

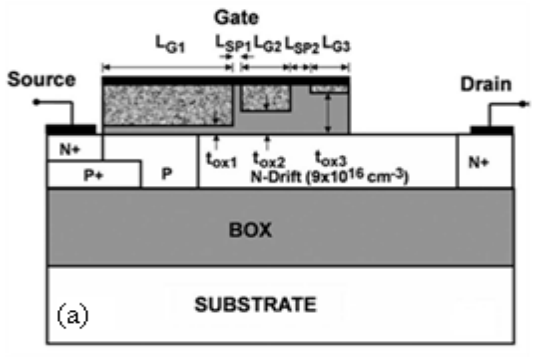
***Keywords*:** Power MOSFET – SOI technology - Laterally double diffused metal oxide semiconductor (LDMOS) - ON resistance - Parasitic BJT - 2D simulation tool.

I INTRODUCTION

Lateral double-diffused metal oxide semiconductor (LDMOS) devices are widely used in power management, smart power integrated circuits for their convenient integration and also in for automotive and switching applications. It is compatible with standard CMOS process technology and is fabricated widely using SOI technology.SOI LDMOS can be fabricated along with low power logic circuitry. [1– 3].

LDMOS used in automotive applications should have a higher breakdown voltage for supporting greater voltage across the drain and the source during the OFF-state and a lower ON-resistance to reduce the power loss. However, obtaining a trade-off between the ON-resistance and the breakdown voltage of an LDMOS is a complex process. A parasitic BJT is present in the LDMOS, which shares its emitter with the source, the base with the channel and the collector with the drain of an LDMOS. The parasitic BJT is turned-ON when the emitter base junction is forward biased due to the accumulation of holes in the channel region. It makes the device breakdown at a lower drain voltage and thus, reduces the breakdown voltage of an LDMOS. Several results have been reported recently to reduce the ON-resistance of the device by various structural modifications [1– 5]. Most popular structural modifications include ESG LDMOS (Extended p^+ Stepped Gate LDMOS)(Fig 1) and Dual channel n-p-LDMOS (Fig 2). These structures probably try to reduce the floating body effect to attain reduced ON- resistance. The floating body or parasitic bipolar effect causes the performance degradation of the device due to impact ionization.

In this paper, we propose to utilize the parasitic BJT to reduce the ON-resistance of the SOI LDMOS by isolating the p^+ of source region as separate contact. There is 26 % reduction in the ON-resistance 8 % improvement in switching speed of BE-LDMOS



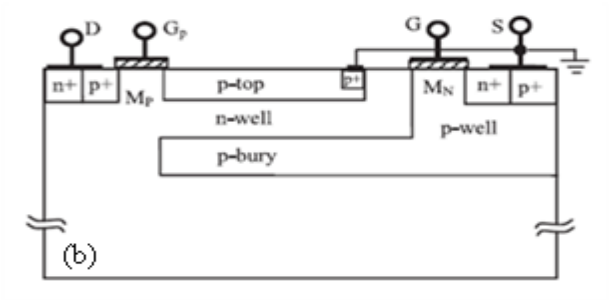


Fig 1.Cross section of ESG LDMOS
Fig 2.Cross section of Dual channel n-p-LDMOS

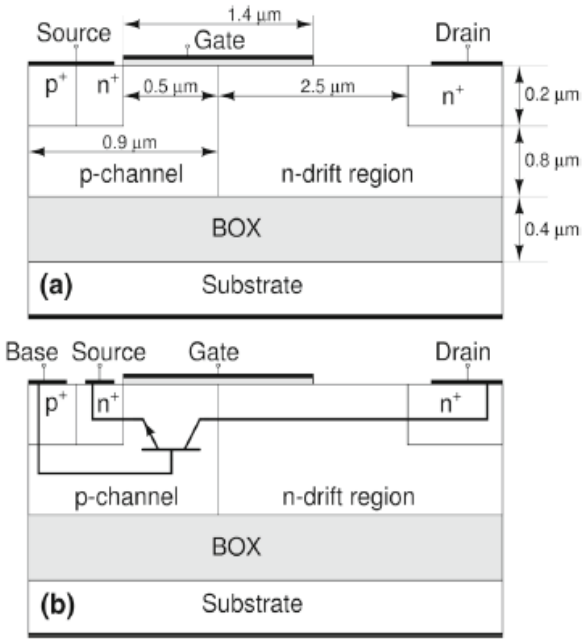


Fig.3 (a) Cross sectional view of conventional LDMOS
(b) Cross sectional view of proposed BELDMOS

II STRUCTURE AND OPERATING PRINCIPLE

The cross sections of the conventional (LDMOS) and the proposed (BE-LDMOS) devices are shown in Fig.3.

Both devices have exactly the same dimensions and the parameters: buried oxide thickness = 400nm, active region Si thickness =1 µm, width of p^+ body, the n^+ source and the drain regions = 0.2 µm, width of the p-body = 0.9 µm, width of the n–drift region = 2.5 µm,gate length = 1.4 µm, gate oxide thickness = 50 nm,n-drift region doping = $2 \times 10^{16}cm^{-3}$, p-channel region doping = $1 \times 10^{17}cm^{-3}$.

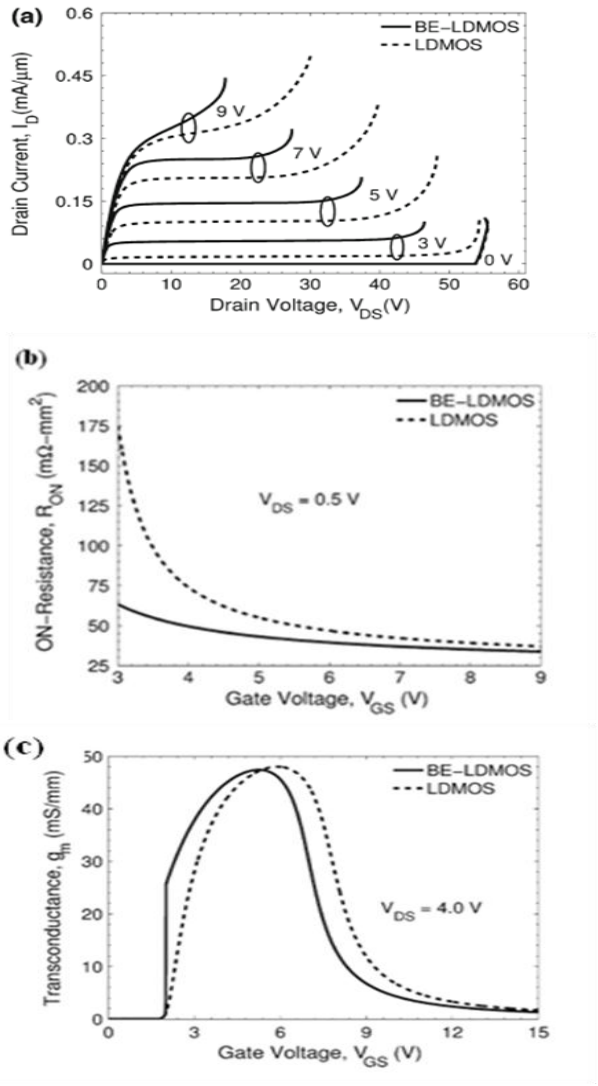
In an SOI LDMOS, the source terminal is connected to the n^+ as well as p^+ body contact to reduce the floating body effect. In BE-LDMOS, the p-channel region, which acts as the base of the parasitic bipolar transistor, has an independent contact without shorting it to the source. Hence, the p-channel acts as the base with the p^+ region as the base contact and the source and the drain regions act as the emitter and the collector of the BJT in the BE-LDMOS, respectively as shown in Fig. 3b. Applying a positive base voltage forward biases the emitter–base junction and turns-ON the BJT. As the collector current increases with an increase in the base–emitter voltage, the total drain current in the BE-LDMOS also increases reducing the ON-resistance for a given gate voltage.

III RESULTS AND DISCUSSION

The simulations are performed using Silvaco's 2D device simulator ATLAS

3.1 Device characteristics

The output characteristics for both the devices are shown in Fig.4a. It can be seen that the BE-LDMOS exhibits more drain current as compared to the LDMOS for a given gate voltage due to the BJT action in BE-LDMOS.. In the channel region of BE-LDMOS, the potential barrier for electrons is lesser as compared to that of LDMOS as the emitter–base junction is forward biased as V_{BS} = 0.7 V. This helps in allowing more electrons to be injected from the source region to the drift region thus, increasing the drain current for a given gate voltage. On-resistance is the resistance between drain and source with a specified VGS applied to bias the device to the on-state. The measurement is made in the ohmic (i.e. linear) region of the device. The ON-resistance versus the gate voltage is shown in Fig. 4b.



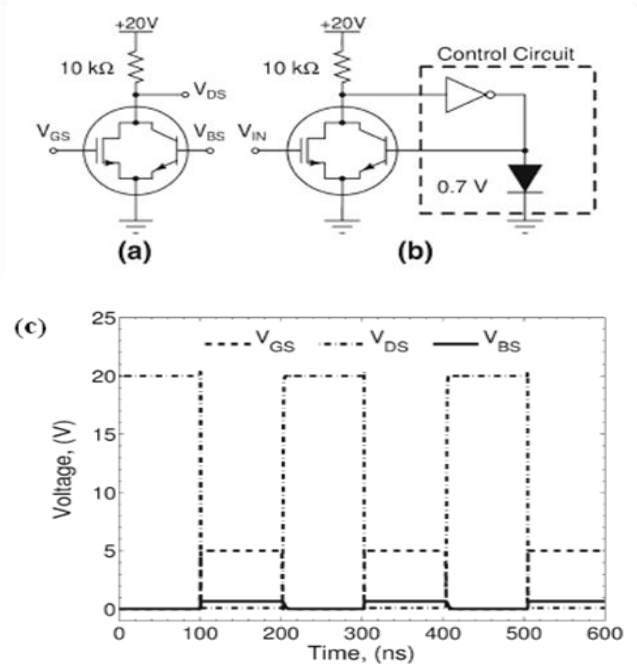


Fig5 (a) BE LDMOS using drain resistance (b) Control Circuit for biasing BE-LDMOS (c) Transient analysis for BE-LDMOS

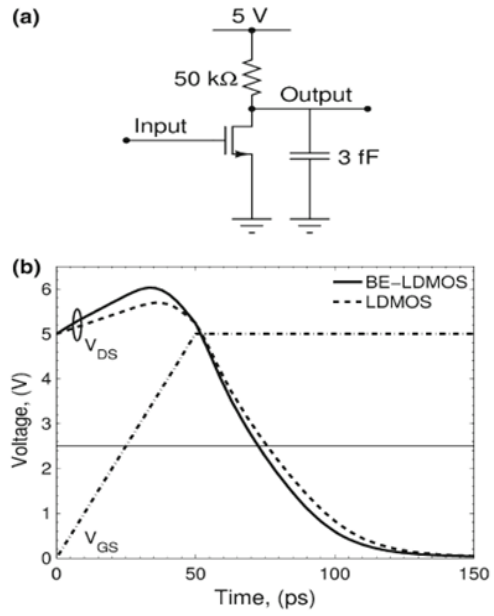


Fig 6(a) Circuit diagram of switching characteristics (b) Switching characteristics comparison

Fig 4. (a) Drain voltage versus drain current for a constant gate voltage (b) ON-resistance versus gate voltage for LDMOS and proposed BE-LDMOS(V_{BS}=0.7V)(c) Transconductance versus gate voltage for LDMOS and BE-LDMOS

There is a 26.2 % decrease in the value of ON-resistance for the BE-LDMOS as compared to the LDMOS. This reduction in the ON-resistance is ascribed to the increase in the drain current of BE-LDMOS due to the BJT action.

Transconductance, an important parameter is the measure of change in drain current with respect to change in gate source voltage at constant drain source voltage. The peak value of transconductance is 47 mS/mm and the range of gate voltage for transconductance higher than 20 mS/mm is approximately 5.5 V for both the devices. These two parameters are almost same for both the devices as shown in Fig. 4c. The off-state breakdown voltage is defined the drain voltage when the drain current is 1×10^{-9}A/μm for V_{GS} = 0 V. It is 54 V for both the devices as shown in Fig. 4a. Due to turning on of the parasitic BJT, the safe operating area (SOA) of BE-LDMOS has decreased .

3.2 Biasing circuit

Adding a base contact to BE-LDMOS makes it a four terminal device. A control circuit has to be designed which forward biases the emitter base junction to turn-ON the BJT when the BE-LDMOS is turned-ON by applying a gate voltage higher than the threshold voltage. The control circuit, shown in Fig. 5b, detects whether the LDMOS is ON or OFF and generates the control signal to bias the base of the parasitic BJT in BE-LDMOS .A single control signal has been used to bias the BJT [4].

A square wave is fed to the gate terminal of a common source circuit as shown in Fig. 5a. The base is also an input in the circuit and output is checked at the drain for two cases mixed mode of Silvaco's ATLAS. The LDMOS remains in the off state when

the gate voltage is 0 V.

For the first case, when the BJT is in OFF-state by biasing the base to 0 V, the drain voltage is 20 V. For the second case, when the BJT is in ON-state by biasing the base to 0.7 V, the drain voltage is 17.5 V.The value of resistance should not be too high. The LDMOS turns-ON by changing the gate voltage to 5 V. The drain current starts flowing and the drain voltage starts decreasing and stabilizes at approximately 0.1 V for both the BJT biasing conditions. When the LDMOS is in ON-state, the drain voltage is approximately 0.1 V and when it is in OFF-state, the drain voltage it is equal to V_{DD}. This change in the voltage can to be detected easily for controlling the base terminal of the BJT.Thus, this circuit can be used to control the parasitic BJT with only one control signal.

3.3 Switching

The switching speed of the device is calculated using a simple inverter configuration as shown in Fig. 6a. The simulation is performed using the mixed mode of Silvaco's ATLAS. The width of both the devices is taken as 50 µm. The input pulse is rising to 5 V in 50 ps and output is checked at the drain across a load capacitor of 3 fF. The base contact in the case of BE-LDMOS is connected using the biasing circuit shown in the previous section. The rise time is taken as the difference in the time when, V_{DS} attains a value of 2.5 V and V_{GS} is at 2.5 V. BE-LDMOS and LDMOS exhibit rise time of 47 and 51 ps, respectively. Thus, BE-LDMOS shows an improvement of 7.8 % in the switching time. This is ascribed to the reduction in the ON-resistance of BE-LDMOS which results in the reduced RC time constant.

IV CONCLUSIONS

Proposed a new BJT enhanced LDMOS (BE-LDMOS) which exhibits 26.2 % reduction in the ON-resistance and 7.8 % improvement in the switching speed as compared to the conventional SOI LDMOS. Use of parasitic BJT affects the safe operating area of LDMOS marginally.

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