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ABSTRACT

This work presents a design of voltage controlled oscillator (VCO) based current to digital converter which is used for sensor readout applications. When we convert the sensed output of current sensor into digital using ADC nonlinearity will occur due to quantization. It can be greatly reduced using Digital IIR filter instead of using an Analog filter. Further first order noise shaping can also be achieved by using the additional filter operations without large power consumption. Proposed architecture designed for an ambient light sensor application, it achieves 900pA accuracy for an input current range of 4µA. The sensor readout architecture consumes only 77.8µA current in the total power, and occupies an active area of 0.36 mm.

Keywords —**Voltage Controlled Oscillator, Analog-to-Digital Conversion, Delta Sigma Modulation, VCO Quantizer, Digital IIR Filter, DAC, Sensor Applications.**

I. INTRODUCTION

An analog-to-digital converter (ADC, A/D, or A to D) is a device that converts a continuous physical quantity (usually voltage) to a digital number that represents the quantity's amplitude.

The conversion involves quantization of the input, so it necessarily introduces a small amount of error. Furthermore, instead of continuously performing the conversion, an ADC does the conversion periodically, sampling the input. The result is a sequence of digital values that have been converted from a continuous-time and continuous-amplitude analog signal to a discrete-time and discrete-amplitude digital signal.

An ADC is defined by its bandwidth (the range of frequencies it can measure) and its signal to noise ratio (how accurately it can measure a signal relative to the noise it introduces). The actual bandwidth of an ADC is characterized primarily by its sampling rate, and to a lesser extent by how it handles errors such as aliasing.

A typical current sensing system consists of a sensor element that produces an output current proportional to the sensed quantity followed by a current (or voltage) to digital converter. Because sensor output is a analog signal, current (voltage) to digital converter is more generally represented as a analog-to-digital converter (ADC). ADC output is typically further processed by a digital signal processor before acting on the information gathered by the sensor. Several techniques were proposed to efficiently convert sensor information to digital output.

Voltage controlled oscillators (VCO) implemented using CMOS inverter-based ring

oscillators to perform accurate current to digital conversion. VCO based ADCs also referred to as VCO quantizers (VCOQ) have recently emerged as an attractive alternative for classical voltage, current or charge-based analog to digital converters. Implemented using mostly digital circuits, they achieve first order noise shaping without using feedback and provide inherent anti-aliasing. However, their performance is severely limited by the non-linearity of VCO's voltage-to-frequency (V-to-F) transfer characteristic. This paper presents a current sensing VCO based ADC architecture that uses synthesized digital logic to tackle V-to-F non-linearity. Designed for an ambient light sensor application, the prototype achieves 900pA accuracy for an input current range of 4µA while consuming 77.8µA quiescent current. Many of the recent research efforts on VCO based ADCs are therefore focused on reducing the impact of V-to-F non-linearity on ADC performance. VCOQ is embedded in a feedback loop and a high gain loop filter was used to suppress non-linearity to the extent of filter gain in the signal bandwidth. To better understand the impact of feedback on non-linearity suppression, it is instructive to evaluate input voltage swing of the VCOQ.

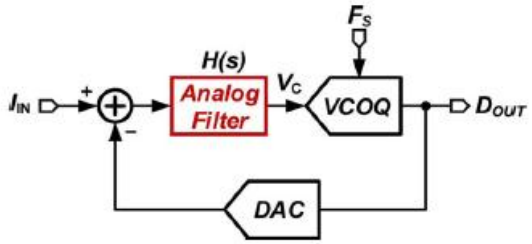

Fig.1 Non-linearity suppression by embedding VCOQ in Feedback loop

II.PROPOSED ARCHITECTURE

A simplified block diagram of the proposed sensor current readout circuit is shown in figure. The difference between sensor output and feedback current ($I_{IN} - I_{DAC}$) is integrated on the intrinsic capacitance of the sensor to generate voltage V_C, which is digitized by VCOQ to produce output digital word D_F. VCOQ output is filtered by the IIR filter and is fed to a DAC, which generates feedback current I_{DAC} Designing the IIR filter to have infinite DC gain ensures the VCOQ output and its input are centered around zero and bias voltage V_{BIAS}, respectively. As a result, VCOQ non-linearity is not exercised, thereby greatly improving the overall linearity of the sensor readout circuit. As a side benefit, the sensor is also biased to voltage V_{BIAS} because $V_C \approx V_{BIAS}$ in steady state. Furthermore, since VCOQ has 1st order noise shaping, the proposed architecture exhibits 2nd order noise shaping, due to the additional filtering provided by H(S).

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The implementation of Digital IIR filter to the architecture is composed of an accumulator and a feed-forward path across the accumulator resulting in a filter transfer function $H_P(Z)$.

$$H_P(z) = \frac{8 - 7z^{-1}}{1 - z^{-1}}$$

Accumulator provides the needed high DC gain and the feed-forward path stabilizes the feedback loop that is otherwise un-stable because of the presence of two integrators: digital accumulator in the IIR filter and passive integrator at the input. The feed-forward path gain is set to 8 considering ease of implementation and the tradeoff between ripple caused on the VCOQ input voltage and modulator stability.

A. Block Diagram

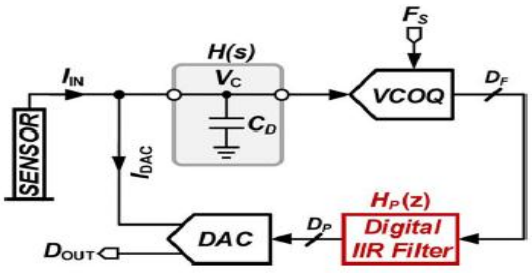

Fig.2 Conceptual Block diagram of proposed VCO based ADC

1.VCO Quantizer

Voltage-controlled oscillator or VCO is an electronic oscillator whose oscillation frequency is controlled by a voltage input. The applied input voltage determines the instantaneous oscillation frequency.

VCO based ADCs also referred to as VCO quantizers (VCOQ) have recently emerged as an attractive alternative for classical voltage, current or charge-based analog to digital converters.

VCOQ are mostly implemented using digital circuits, they achieve first order noise shaping without using feedback and provide inherent anti-aliasing.

It consists of a transconductor (G_M) that converts the difference between sense node voltage V_C, and bias voltage V_{BIAS}, into current and feeds it to the current-controlled oscillator (CCO). Using the front-end G_M stage as depicted, instead of controlling the VCO directly with V_C, offers flexibility in appropriately biasing the sensor. In steady state, because DC gain of the IIR filter is infinite $V_C = V_{BIAS}$, resulting in the sensor to be biased at V_{BIAS}. Further, V_{BIAS} can be set to any voltage within the input common-mode range of the G_M stage.

$$V_C = \frac{H(S)}{1 + H(s)A_{VCO}(s)A_{DAC}(s)} I_{IN}$$

Here VCO Quantizer uses the counter based FDC. Counter-based FDC measures frequency by taking the difference between the numbers of VCO cycles in two consecutive cycles of the 160 kHz sampling clock. As a result, F_{VCO} can be much larger than F_S.

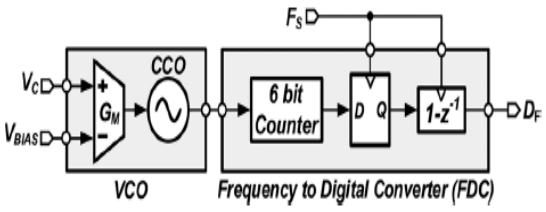

Fig.3 VCO Quantizer with FDC

2. FDC

Analogous to the PFM type readout architecture, the sensor output voltage is converted to frequency, by a VCO and digitized using an FDC.

An FDC is most commonly implemented using a set of flip-flops and an XOR gate. Flip-flop FF1 acting as a phase detector samples and quantizes VCO output phase at a sampling rate of , while FF2 and XOR gate perform digital differentiation of the quantized VCO phase to generate digital output.

Wide-bandwidth systems often require high-performance frequency-to-digital converters (FDC) so as to optimize the operating conditions of the system to be suitable for the frequency range of the system clock before the normal operation begins. This can be usually done with a digital code containing the operating frequency information of the system clock.

Counter based FDC is used instead of XOR based FDC architecture. A counter-based FDC measures frequency by taking the difference between the number of VCO cycles in two consecutive cycles.

The counter counts the number of positive (or negative) edges of the VCO output clock for the duration of one sampling clock cycle and stores it in a register. The stored count is a measure of the accumulated phase at the end of that clock cycle. A digital differentiator is used to subtract consecutive stored count values to determine the frequency information in digital form.

3. Digital IIR Filter

In signal processing, a **digital filter** is a system that performs mathematical operations on a sampled, discrete-time signal to reduce or enhance certain aspects of that signal. The non linearity of the voltage-to-frequency conversion is tackled by using Digital IIR filter.

A digital filter system usually consists of an analog-to-digital converter to sample the input signal, followed by a microprocessor and some peripheral components such as memory to store data and filter coefficients etc. Finally, the digital-to-analog converter is used to complete the output stage. In some high performance applications, an FPGA or ASIC is used instead of a general purpose microprocessor, or a specialized DSP with specific paralleled architecture for expediting operations such as filtering.

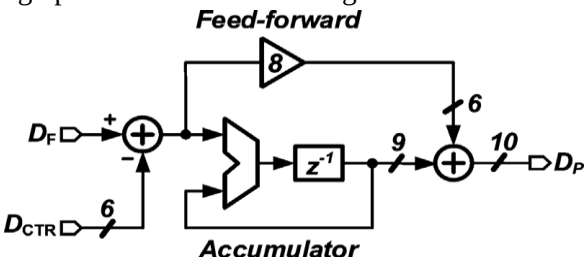

Fig.4 Digital Filter Architecture

It is composed of an accumulator and a feed-forward path across the accumulator resulting in a filter transfer function $H_P(Z)$ equal to:

$$H_P(z) = \frac{8 - 7z^{-1}}{1 - z^{-1}}$$

Accumulator provides the needed high DC gain and the feed forward path stabilizes the feedback loop that is otherwise unstable because of the presence of two integrators: digital accumulator in the IIR filter and passive integrator at the input. The feed-forward path gain is set to 8 considering ease of implementation and the tradeoff between ripple caused on the VCOQ input voltage and modulator stability.

4. Feedback DAC

Feedback DAC is used in the VCO based ADC design. Since the IIR filter output D_P, is 10 bits long, using a Nyquist-rate DAC requires a large number of very small unit elements. To avoid this, 10 bit D_P is truncated to 9 levels using a 1st order digital$\Delta\Sigma$ before feeding it to a 9-level current-mode DAC.

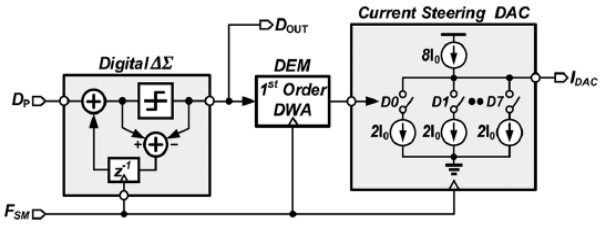

Fig.5 Architecture of the Feedback DAC

The truncation error introduced by the $\Delta\Sigma$modulator is made lower than the FDC quantization error by clocking it at 2.56 MHz, which is 16 times faster than F_S. The $\Delta\Sigma$modulator is implemented using error-feedback architecture. Dynamic element matching (DEM) implemented using 1st order data weighted averaging (DWA) algorithm is used to suppress DAC unit element current mismatch errors. The DAC unit elements are sized for 8 bit matching and the DWA improves the linearity to more than 12 bits. Because excess loop delay (ELD) in the feedback path is negligible (approximately equal to $1/F_{SM}$) compared to the clock period ($1/F_S$), stability is not compromised and hence ELD compensation is not needed in this design. The entire digital section of the VCOQ is synthesized using standard place and route tools.

Delta-sigma (**ΔΣ**; or **sigma-delta**, **ΣΔ**) modulation is a method for encoding analog signals into digital signals as found in an ADC. It is also used to transfer higher-resolution digital signals into lower-resolution digital signals as part of the process to convert digital signals into analog.

5. Dynamic Element Mismatching

Many practical DAC architectures use switches and matched components to convert signals. In practice, perfectly matched components are not possible due to fabrication limitations, thermal gradients, component aging and component noise. The difference between the actual component value and the actual component value is called mismatch error.

DEM techniques dynamically rearrange the interconnections of mismatched components so that the time averages of the equivalent components at each of the component positions are nearly equal. If the interconnections are varied such that the mismatched components' virtual positions are sufficiently varied, the harmonic distortion caused by the mismatched components can be reduced, frequency shifted or eliminated. Therefore, DEM techniques can increase a DAC's SFDR, SDR, SNDR and ENOB.

Deterministic DEM techniques and stochastic DEM techniques have been developed for DACs. Deterministic DEM techniques, such as clocked level averaging, data weighted averaging, and individual level averaging, improve DAC performance by locating the distortion caused by the component mismatch errors in certain frequency bands. This distortion is reduced or removed in subsequent processing such as low pass filtering in DS architectures. Stochastic DEM techniques, such as stochastic level averaging, randomly permute DAC circuit components each sample. Unlike deterministic DEM techniques which generate harmonic distortion, stochastic DEM techniques can spread the mismatch error energy across the spectrum generating white or colored noise in the DAC output.

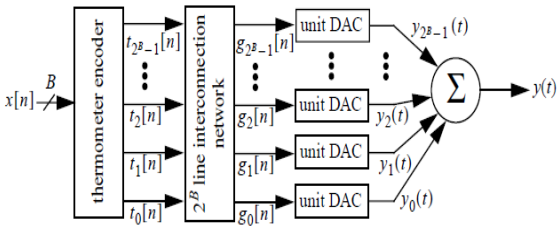

Fig .6 A B bit Dynamic Element Matching DAC Architecture

Table1. Comparison Summary

Parameters	Proposed systems	Conventional system
Architecture	Mostly Digital	Analog
Technology (nm)	180	180
VDD (V)	5/1.8	1.8
IQ (µA)	77.8	1300
Area (mm2)	0.36	1.26
Input Type	Current	Current
Input Range	1 to 4000nA	0.004 to 21nA
Accuracy	0.9nA	0.004nA
Dynamic Range (dB)	73	77

III. CONCLUSION

The Digital IIR filter to improve the linearity of the VCO based ADC architecture. It is achieved by the feed forward path and accumulator. The accumulator provides infinite DC gain and the feed-forward path introduces a loop zero and stabilizes the overall feedback loop. However, use of an accumulator increases the number of bits fed back to the DAC, which necessitates a large number of DAC unit elements. The DAC unit is implemented using Delta Sigma modulation to reduce the hardware complexity. The proposed model achieves a gain and offset corrected accuracy of 900 pA in an input range of 4 A. The full scale input current is limited by the maximum DAC current. The total current consumption is 77.8 A out of which 62.5 A is consumed from the 5 V supply and 15.3 A from the 1.8 V supply. The 5 V supply used for the analog sections can be reduced down depending on the application, which will further improve the power efficiency. Further improvement in linearity can be made by replacing the Digital filter into Active filter.

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