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Design of Low Power, Low Area and High Performance Hybrid -Type CAM using Fin-FET Technology

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ABSTRACT

Power dissipation due to memories has become a major concern of modern digital design. The conventional CMOS technology has a major problem of short channel effects. So, the CAM cells are designed using FinFET technology which has better gate control over drain to source current. The CAM has a parallel active circuitry which consumes more power and the main challenge in designing the CAM is to reduce the power consumption without reducing the speed and memory density. This project proposes a hybrid-type CAM for the advantage of speed and performance of the system and the results are compared with conventional CAM cell.

Key Words— *Content Adderssable Memory (CAM), Hybrid-Type CAM, high performance, low area, low power, searching, SRAM.*

I. INTRODUCTION

In CAM, the input is associated with the data stored in the memory and output is the location where the content is stored. CAM can be used as a search engine for finding the matched contents in a database or a table. In CAM applications, where more than one word is matched, a priority encoder is used. In order to access a particular entry in such memories, a search data word is compared against previously stored entries in parallel to find a match. Once a search data word is applied to the input of a Content Addressable Memory, the matching data word is retrieved within a single clock cycle if it exists [1].

This prominent feature makes CAM a promising candidate for applications such as frequent and fast look-up operations, network routing, cache coherence, and novel models of computation. Although dynamic CMOS circuit techniques [6] can result in low-power and low-cost CAM's, these designs can suffer from low noise margins, charge sharing, and other problems not to be energy efficient when scaled.

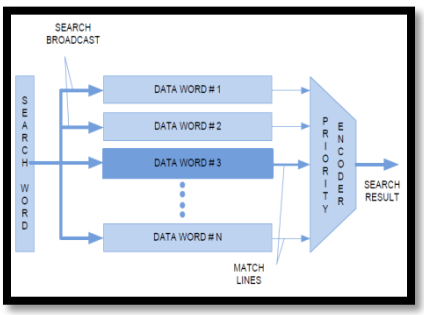

Figure 1. Content Addressable Memory

Thus a new associative CAM memory called hybrid-type CAM has been recently introduced and implemented using FINFET technology. In this paper, shorted gate FinFET is used in which the two gates are shorted together to give high current drive.

The rest of this paper is organized as follows. Section II describes the basic CAM cell. Section III describes the FINFET Modes And Device Model Parameters. Section IV describes about the proposed Hybrid-Type CAM cell. The conclusion is given in Section V.

II. BASIC CAM CELL

A. OVERVIEW OF CAM AND RAM

The RAM has two major operations: Write and Read. (i.e.) user supplies the memory address and the RAM returns the data stored in that address. A CAM has three major operations: Write, Search and Read.(i.e.)user supplies the data word and CAM search its entire memory to see the supplied data word. If the data word is found, the CAM returns one or more storage address where the word was found [7]. CAM is used in various application like IP Packets in network routers, Broad ATM communication system and Image coding.

B. BASIC OPERATION OF CAM CELL

The CAM mainly consists of an array of memory cells. Each cell has two units, store unit and compare unit. The store unit, which uses Cross-Coupled 6T SRAM, is used for storing the bit. The compare unit made of pass transistor logic is used to compare the search bit and stored bit. The CAM cell can be of either XOR or XNOR type as shown in Figure 2. The output of compare unit is fed to gate terminal of pull-down transistor N5. Based on the output of compare unit, the transistor may turn ON or OFF. Match line is connected to the pull-down transistor. If the transistor is ON (OFF), the match line discharges (charges)2. Conventionally, there are two types of CAM designs: NOR type and NAND type. In any CAM design, there are two phases precharge and evaluation. In precharge phase, the match line is charged to high voltage level and in evaluation phase, the data in store unit and compare unit are compared.

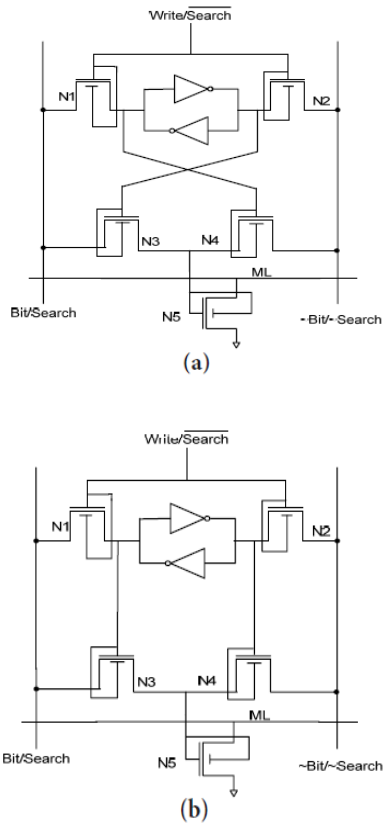

Figure 2. Typical CAM Cell. (a) XOR type. (b) XNOR type.

III. FINFET MODES AND DEVICE MODEL PARAMETERS

The continuous down in scaling of bulk CMOS creates major issues due to its base material and process technology limitations. The main drawback of CMOS based design is the leakage in small channel size; due to this the leakage stems increased from the lower oxide thickness, more substrate dopings [2]. The optimal performance of the device can be achieved by lowering the threshold voltage with low supply voltage worsen the leakage.

The primary obstacles to the scaling of CMOS gate lengths to 22nm and beyond includes short channel effects, sub-threshold leakage, gate-dielectric leakage and device to device variation reduction which leads low yield.

The FINFET based designs are known as double gate device which offers the better control over short channel effects, low leakage current and better yield in 22nm and beyond which helps to overcome the obstacles in scaling When threshold voltage Vt is less than a potential voltage, gates of the double gate or FINFET device activates the currently flow between drain to source with modulating the channel from both the sides instead of one side. The potential which is applied to two gates together influence potential of the channel which fighting against the drain impact and leads to solve and give the better shut off to the channel current and reduces Drain Induced Barrier Lowering (DIBL) with improved swing of the design [5]. This FINFET based transistors offers good trade off for power as well offering interesting delay. The Figure 3.1 shows the 3D structure of multi-FIN based field effect transistors.

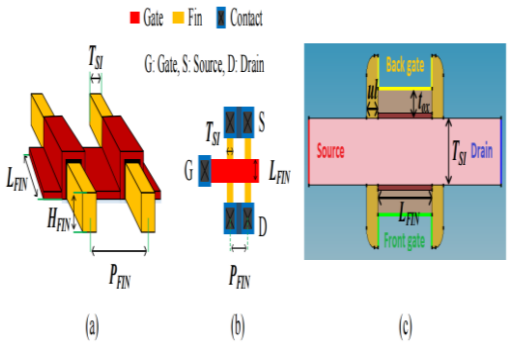

Figure 3.1 (a) Structure (b) layout of a FinFET device with two fins (c) 2D model of 7-nm FinFET devices in TCAD.

A. Modes of FINFET

Double Gate (DG) devices have been used in a variety of innovative ways in digital and analog circuit designs. A parallel transistor pair consists of two transistors with their source and drain terminals tied together. In Double-Gate (DG) FINFETS, the second gate is added opposite to the traditional gate, which has been recognized for their potential to better control short channel effects, as well as to control leakage current. The modes of FINFETs are identified as short gate (SG) mode with transistor gates tied together, the independent gate (IG) mode where independent digital signals are used to drive the two device gates, the low-power (LP) mode where the back-gate is tied to a reverse-bias voltage to reduce leakage power and the hybrid (IG/LP) mode, which employs a combination of low power and independent gate modes. Here independent control of front and back gate in DG FINFET can be effectively used to improve performance and reduce power consumption [8]. Independent gate control is used to combine parallel transistors in non-critical paths.

B. FINFET Device Modelling Parameters

The FINFET is originally known as the folded channel MOSFET which has narrow vertical fins from wafer. Usually width of the gate will be double of the fin height in FINFETs [2]. FINFETs are nominated instead of CMOS in less than 22nm technology due to its cost effective manufacturing.

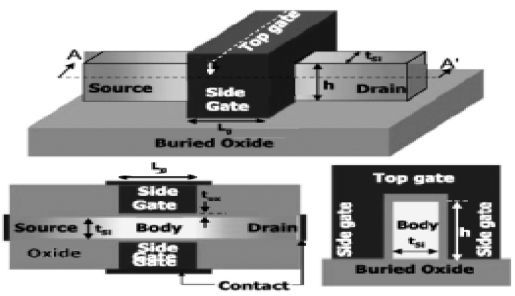

Figure 3.2 Modeling parameters of FINFET

The geometric key parameters of FINFETs are

- Lg – Length of the gate,
- h – Height of the FIN,
- tox – Thickness of gate oxide,
- tox-top - Oxide thickness of top gate and fin,
- Tsi- Thickness of the fin
- Channel Doping.

These parameters are playing an important role in minimizing the Ioff leakage current and maximize the *Ion* current. Height of the fin should be same all over the chip to avoid the process complications and reduce the defects. Height balancing, thickness of fin, thickness of oxide and channel length should be balanced based on the FIN engineering. The Figure 3.2 shows the modeling parameters of FINFETs. The Table 3.1 shows the comparison of device parameters for nominal 22nm FINFET and CMOS NMOS and PMOS devices.

Table 3.1 Properties of FINFET and CMOS device

DEVICE PARAMETERS	FINFET		CMOS	
	NMOS	PMOS	NMOS	PMOS
Gate Length (L_g)	22 nm	22 nm	22 nm	22 nm
Thickness of Fin and channel (t_{si})	8 nm	8 nm	8.6 nm	8.6 nm
Thickness of oxide (t_{ox})	1.05 nm	1.1 nm	1.4 nm	1.4 nm
Height of the Fin	16 nm	16 nm	-	-
Channel doping (cm^{-3})	10^{16}		$4x10^{18}$	
Supply voltage	0.8 V		0.9 V	

HYBRID-TYPE CAM CELL

Hybrid-type CAM used to improve performance, speed and area of the system using FinFET technology. Hybrid-type CAM design consists of both NOR-type array with XOR CAM cell for performance advantage and NAND type array with XNOR CAM cell for power advantage.

Mainly we divide the complete circuit into 3 parts namely, SEG1, SEG2 and CONTROL circuitry. In the SEG 1, we design the circuit using XNOR type and then arrange the pulldown transistors using NAND-type. In the SEG 2, we design the circuit using XOR type and the pull-down transistors are arranged in NOR type. Both array has the advantages of performance and power of the system [3].

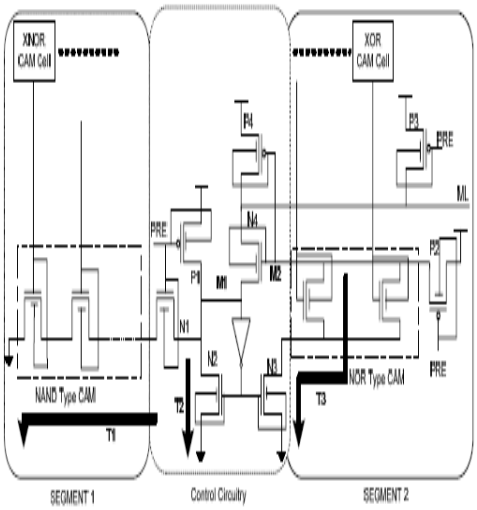

Figure 4.1 Hybrid-Type CAM Structure

Hybrid-type CAM structure consists of SEG1, SEG2 and CONTROL circuitry. In SEG 1, the circuit is designed using XNOR type and then the pull-down transistors are arranged using NAND-type. In SEG 2, the, the circuit is designed using XOR type and then the pull-down transistors are arranged using NOR-type. The Hybrid-type CAM structure is shown in Figure 4.1.

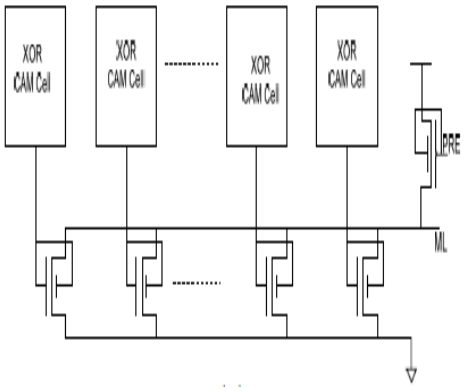

Figure 4.2. NOR Type CAM array

The NOR-type CAM design, the CAM cell is usually XOR-type, and the pull-down transistors of each CAM cell are arranged in NOR type. During precharge phase, the match line is initially precharged to high.

In contrast to the NOR-type CAM, the NAND-type CAM aims to reduce the power dissipated in search operation, in which the CAM cell is implemented as XNOR-type instead of XOR-type, and the pull-down transistors of each CAM cell in the same word are arranged in NAND type. The match line is initially precharged to high, and discharged to 0 only when all CAM cells are matched.

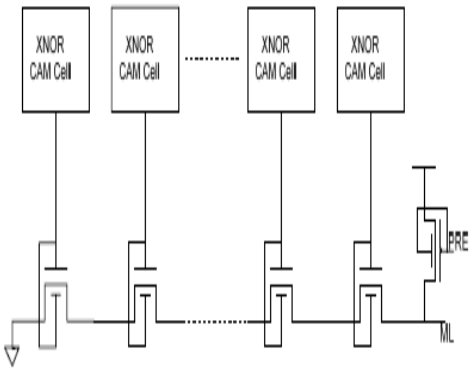

Figure 4.3. NAND Type CAM array

Search Operation of Hybrid-type CAM Cell

In case of searching a data, the input data is compared with that of stored data. The search operation of CAM cell is performed in two phases.

- ML precharge
- ML evaluation.

In ML precharge phase, match line is charged to high and then in ML evaluation phase based on the match and mismatch of the words the match line will change the logic from high to low or low to high.

ML Precharge Phase

During the precharge phase, the PRE signal is low and the Match Line (ML) is charged to high through P3. In Fig 4.2, T1, T2 and T3 are the pull-down paths in the circuit. The M1 node is at high because of transistor P1, which drives the transistors N2 and N3 OFF due to which the path T2 and T3 are disconnected from ground. The low PRE signal turns OFF transistor N1. Therefore all the pull-down paths are disconnected.

ML Evaluation Phase

During evaluation phase, the PRE signal is high and the search bits are loaded on bit lines. The hybrid-type CAM is divided into two segments SEGMENT-1 (SEG_1), and SEGMENT-2 (SEG_2) as shown in the Fig 4.2. When two segments have match, then match line will discharge through any one of the pull-down paths. When we search the data we come across 4 different cases but the exact matching occurs only when both the segments are matched. The voltages of each node are shown in Table 4.1

	SEG 1	SEG 2	Path			Key Node			Result
			T1	T2	T3	M1	M2	ML	
Case 1	Mismatch	Mismatch	X	X	X	H	H	H	Mismatch
	Mismatch	Match	X	X	X	H	H	H	Mismatch
Case 2	Match	Mismatch	0	0	0	L	L	H	Mismatch
Case 3	Match	Match	0	0	X	L	H	L	Match

Table 4.1: Node Voltages of each node of Hybrid-type CAM Cell

Case i):

In this case, the SEG1 is mismatched and SEG2 is mismatched or matched. Since the SEG1 is mismatched there exists no discharge path because there may be at least one transistor that is OFF. So the node voltage M1 remains HIGH. Thus in this case the matching process does not depend on the SEG2. Since there is no discharge path the Match-line still remains in the HIGH state.

Case ii):

In this case, SEG1 is matched and SEG2 is mismatched. As the SEG1 is matched all the transistors that are connected in the NAND fashion are in ON state, so that there exists a discharge path through the path T1. And thus, the node M1 remains LOW and the two pull-down transistor P5 gets ON and so, there exists a path T2 to discharge. Now as the SEG 2 is mismatched there exists at least one path to discharge through N3 so that the node M2 remains LOW. Hence in this case, there won't be any path to discharge the match-line.

Case iii):

In this case, both the segments are matched. Thus, as the SEG1 is matched, the node M1 gets LOW value as there exists a discharge path. Now in case of SEG2, as it is matched all the transistors are turned OFF and the path T3 to ground is disconnected. Now the node M2 is at HIGH state making the transistor N4 to turn ON. Now there exists a path for Match-line to discharge the data, through the paths T1 or T2. As the path T2 is the fastest path to discharge the data, the Match-line discharges through the transistor P5. Thus it indicates that the data have been matched properly. In this design as we have two pull-down paths to discharge the match-line. It discharges through path T2 as path T1 has transistors connected which takes long time to discharge. Thus, this design provides better performance.

IV. CONCLUSION

Thus, a Hybrid type CAM Structure has been designed for Low Power and High Performance using NOR and NAND type CAM Array and area of the complete system has been reduced by replacing 9T basic CAM cell with 4T CAM cell with a fast pull down path to accelerate the search operation.

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