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ANALYSIS OF SRAM WITH LOW-VOLTAGE AND LOW-LEAKAGE POWER USING FINFET

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ABSTRACT

Low power consumption in memory plays an important part in VLSI. But the memory consumes more power. The sub-threshold leakage power is the main reason for high power consumption. Proposed FIN type Field Effect Transistors (FinFET) based 10T SRAM cell is designed to reduce the leakage power compared with conventional CMOS based 10T Static Random Access Memory (SRAM) cell. FinFETs are used as a substitute for bulk CMOS in nanoscale circuits. Independent control of FinFET gates can be used effectively to reduce total active power consumption in digital circuits.

Key Words— *Bulk CMOS, FIN type Field Effect Transistor (FinFET), low power, memory, static random access memory (SRAM)*

I. INTRODUCTION

SRAM is a critical component in many of the digital systems, from high-performance processors to mobile-phone chips. Density, power, and performance are the essential parameters for all applications. SRAM is semiconductor memory cell. It is used to store one bit of information. It is much faster and consumes very less power as compared to other memory cells [1]. In battery-operated portable device power consumption is being the major concern. The major role of power consumption is observed in SRAM as it remains to be in idle mode for some time which in turn produces leakage power in the devices. By scaling of device dimensions leakage power is increased. Thinner gate-oxides can improve Short Channel Effects (SCEs) but it leads to increased gate leakage. For this different transistor structures have been analyzed to replace MOSFET devices and among them FinFETs show better results.

FinFET are double-gate devices which become a popular device candidate for future generations of CMOS technology [2]. FinFET has two gates which can be independently controlled to reduce transistor count and leakage current and it is shorted for higher performance. In FinFETs there will be reduced short channel effects, leakage current and has better scalability [3].

The rest of this paper is organized as follows. Section II describes the comparison of conventional CMOS and FinFET. Section III describes the leakage current reduction techniques for SRAM cell. Section IV gives explanations about FinFET technology. Section V presents the proposed FinFET based 10T SRAM cell. The conclusion is given in Section VI.

II. COMPARISON OF CMOS AND FINFET

The main reason for power dissipation in MOSFET is SCEs and leakage current. When there is high electric field across a thin gate oxide layer there will be penetration of electrons this will result in leakage. When there is decreased separation between depletion regions at the drain-substrate and the source-substrate junctions a punchthrough leakage occurs.

By using CMOS certain low power design techniques are implemented inorder to overcome power dissipation [4]. By reducing the supply voltage, power dissipation can be reduced. But this has a disadvantage of increasing the delay. When the threshold voltage is reduced it increases leakage current and by lowering the capacitance it affects the system performance.

Front and back gates are electrically coupled so SCE can be controlled. In FinFET devices there will be reduction in standby power which is more suitable for low-power designs while simultaneously providing increased performance [5]. The low power techniques that are used for FinFET circuits effectively reduce the circuit power.

SRAM Design Tradeoffs

1. Read and Write Stability

The minimum voltage that is attained during read operation is called as read voltage. Read voltage is the division of voltage between pull down transistor and access transistor. Read stability can be established by low access transistor driving strength which decreases the read voltage.

The maximum voltage that is attained during write operation is called as write voltage. The by division of voltage between pull up transistor and access transistor is the write voltage. Write stability can be established by strong access transistor driving strength which decreases write voltage.

2. Area and Yield

In memory design density and functionality is more important. For large memories functionality is achieved by providing good noise margin between the outputs. The noise margins can be reduced by proper sizing of the device. Based on threshold voltages and supply voltage the functionality can be improved. Density of memory is reduced by increasing size of transistors which results in increased cell area.

3. Speed and Leakage Current

In order to increase the speed of operation and cell performance of SRAM cell low leakage power is much more important. By providing low threshold voltage the speed of SRAM cell can be increased but the leakage power of the device can also be increased. Speed and leakage power is increased by scaling of voltage which results in less threshold voltage. High threshold voltage can be used to reduce leakage power but it affects the performance of the device.

Features of FinFET

For designing of SRAM cell the following features of FinFET are more suitable.

- Thin body of FinFET reduces SCE.
- Less doping gives better carrier mobility, gate leakage currents and device reliability.
- When it is operated at lower voltage there will be less threshold voltage.
- Front and back gates are separated which allows improved control over the channel current.
- For conventional planar transistors it is difficult to scale effectively even when high-k gate dielectrics are used.

III. LEAKAGE CURRENT REDUCTION TECHNIQUES

1. Dual threshold technique

The higher threshold is used at one side and low threshold is used on other side of the circuit. Fig.1 shows circuit diagram of dual threshold 6T SRAM cell.

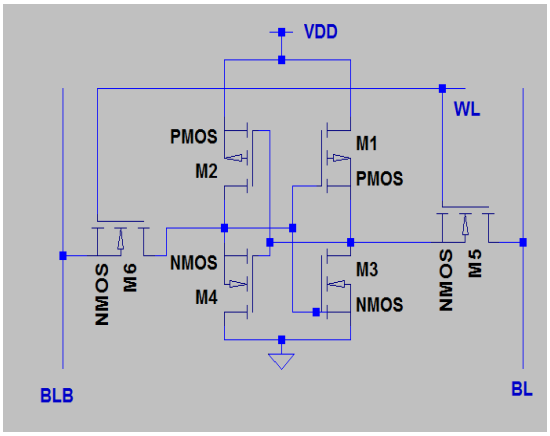

Figure 1 Dual threshold 6T SRAM cell

The low threshold is used at the driving transistors M5 and M6. Switching time will be reduced due to thin channel device, which provides fast access of the cell. M1, M2, M3 and M4 transistors uses high threshold which has thick channel so

they hold low subthreshold leakage current [6]. Low power operation is possible because of less leakage current in SRAM cell.

2. DRG (data retention gated ground) scheme

Fig.2 shows circuit diagram of DRG SRAM cell. Word line (WL) provides gate control signal. Before starting of the read operation particular row of cells will turn "ON" and the remaining rows of cells are inactive so no need to turn "OFF" the whole block. When the cell is inactive, it retains its data with "1" storage node remaining at VDD and "0" storage node lying to an intermediate voltage of the NMOS transistor.

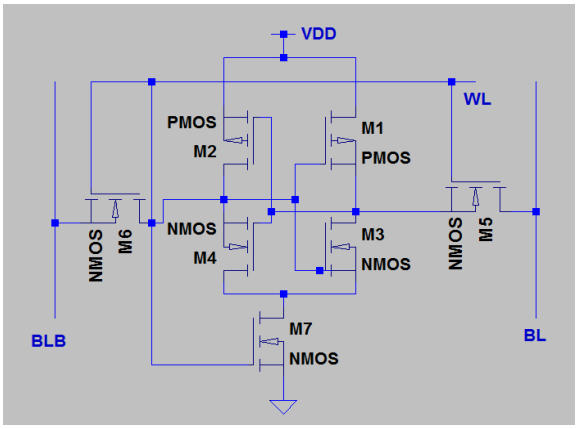

Figure 2 DRG SRAM cell

When the gated transistor turns on the "0" node returns to ground and discharges one of the bit lines. The value stored in the SRAM cell can be retained till the gating transistor is "OFF". There should be proper size of gating transistor.

IV. FINFET TECHNOLOGY

FinFET is a non-planar device and it is "fin" like shaped where the gate is covered over the fin which acts as a transistor channel. It is also termed as quasiplanar double gate transistor as the current flows parallel to wafer plane and the channel is perpendicular to wafer plane Fig.3 shows circuit diagram of structure of FinFET.

Basically, FinFET was designed to be constructed on silicon-on-insulator (SOI) wafers. Now-a-days FinFETs are used to work on bulk silicon wafers to improve the performance of certain parameters [7].

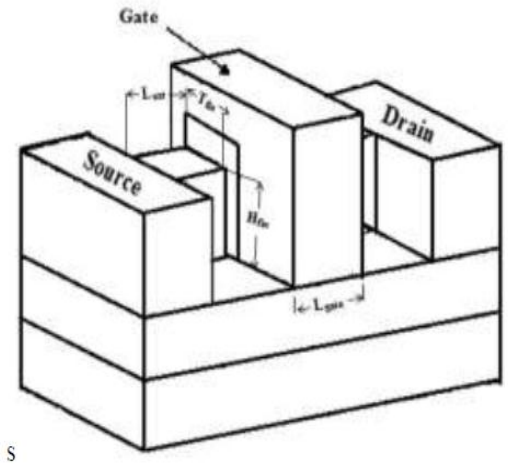

Figure 3 Structure of FinFET

- Effective channel length of the device (L_{eff}) = $L_{gate} + 2\times L_{ext}$
- Effective channel width of the device (W) = $T_{fin} + 2\times H_{fin}$

Where H_{fin} and T_{fin} are the Fin height and thickness respectively. Length of the gate is termed as L_{gate} and extended source or drain region is termed as L_{ext}. Width of the device (T_{fin}) is important for controlling the short channel effect.

So $T_{fin} \sim L_{gate}/2$ is used.

The various logic design styles for designing FinFETs are

Shorted-gate (SG) mode

In this mode both gate are shorted and it avoids SCE due to superior gate to channel coupling.

Independent-gate (IG) mode

In this mode two gates are controlled independently, this reduces the number of transistors in the circuit and also improves design flexibility [8].

Low-power (LP) mode

In this mode low voltage is applied to n-type FinFET and high voltage is applied to p-type FinFET. The threshold voltage of the devices is varied which reduces the leakage power dissipation by increasing delay.

Hybrid IG/LP mode

This is the combination of both IG and LP modes.

FinFET Structure

An ultra-thin Si fin forms a conducting channel in FinFET structure in which the electrons are flow from source to drain. This conducting channel is covered by gate where the input voltages are supplied. The flow of electrons is controlled in off state this prevents the leakage of current. Sometimes there is an increased amount of charge carriers and the breakdown of the conducting channel depends on the flow of charge carriers formed by single fin.

The flow of electrons is blocked from source to drain which stops the current flow. In Multi-Gate Field Effect Transistors (MuGFET) the number of fins are increased which are formed parallel to each other and improves SCE [9]. The amount of charge carriers which flow from higher potential to lower potential is increased when the number of fin are increased. Therefore, the rate at which the carriers flow is faster increasing the switching speed. It has better gate control over the conducting channel it is one of the advantage of multiple fins. Due to this, there is a reduction in current leakage. This attains high on state drive current.

V. FINFET BASED 10T SRAM DESIGN

The SRAM cell is one of the promising application of FINFET based design. The read and write delays are very long in the subthreshold region of the CMOS based SRAM cell. It is one of the problem in CMOS based SRAM design.

CMOS based SRAM cell is exposed to noise while reading. To overcome these problems, FinFET based 10T SRAM cell is designed which is shown in Fig.4. Device sizing is much more important for read stability and write ability. It is necessary to improve the performance of the cell and to improve the read SNM

Write operation

During write operation, the Write Word Line (WWL) is set to high and Read Word Line (RWL) is set to low. Then the data to be written is loaded on BitLine (BL) and BitLineBar (BLB) through write driver.

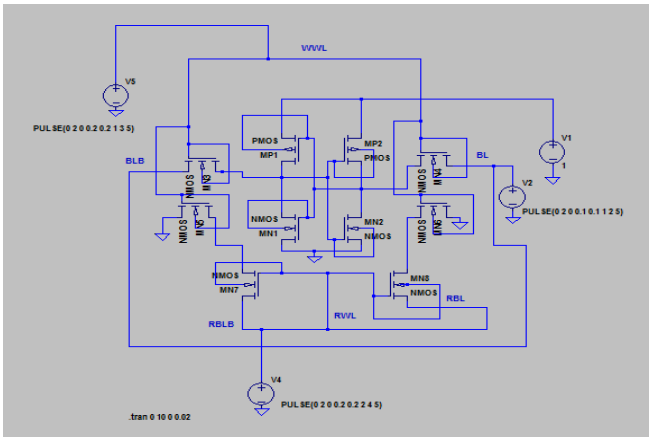

Figure 4 10T SRAM cell using FINFET

Read operation

During read operation, the RWL is set to high and WWL line is set to low. BL and BLB are precharged to V_{dd}. As the WWL line is set to LOW, the write access transistors such as MN3 and MN4 are in OFF state. The BitLine dischargers either MN5 or MN6 will conduct depending on the cell content. BitLine discharger will discharge either BL or BLB through the read access transistors MN7 or MN8.

VI. CONCLUSION

FinFET based 10T SRAM cell is designed to reduce leakage power and SCE. FinFET based circuits has high speed of operation and lower power consumption. Application of FinFET on nanoscale devices shows improved performance over conventional CMOS.

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